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| 6 | D chandra Mouli | EE 7640509 | 21 | 982 | 99.9 |
| 7 | Ashish Kumar Nanda | EE 1620466 | 31 | 912 | 99.86 |
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| 5 | Naveen Kumar K | EC1500400 | 18 | 914 | 99.96 |
| 6 | V. Gopala Krishna Murthy | EC1320585 | 18 | 914 | 99.96 |
| 7 | Nikhil M Duragkar | EC1500054 | 24 | 894 | 99.94 |
| 8 | K Naveen Kumar | EC1580156 | 26 | 890 | 99.94 |
| 9 | M. Kartheek | EC7630362 | 29 | 882 | 99.93 |
| 10 | Chandra sekhar Reddy | EC7640504 | 33 | 874 | 99.93 |
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| 12 | Md Asif Sheik | EC7290318 | 43 | 855 | 99.9 |
| 13 | K.Subhasini | EC1410519 | 43 | 855 | 99.9 |
| 14 | M. Mahender | EC1520240 | 46 | 847 | 99.89 |
| 15 | A. Santhosh Kumar Reddy | EC1470246 | 46 | 847 | 99.89 |
| 16 | M.Sreenivasulu | EC1400672 | 46 | 847 | 99.89 |
| 17 | Kameshwar Atchutaram | EC1460676 | 55 | 839 | 99.87 |
| 18 | MD. Musharaf ali Faruqui | EC1590628 | 55 | 839 | 99.87 |
| 19 | S. Dev Sekhar | EC7620512 | 60 | 835 | 99.86 |
| 20 | Hari Kiran M | EC1400420 | 63 | 831 | 99.85 |
| 21 | N.Kondal Reddy | EC1470572 | 63 | 831 | 99.85 |
| 22 | V. Anil Kumar | EC6860302 | 73 | 815 | 99.83 |
| 23 | Bojja Sandeep Kumar | EC1590626 | 76 | 811 | 99.82 |
| 24 | Ch Srikanth Raj | EC1440189 | 79 | 807 | 99.81 |
| 25 | Hintendra sharma | EC8190306 | 83 | 803 | 99.81 |
| 26 | Shreyan Parakh | EC6660519 | 85 | 795 | 99.8 |
| 27 | M. Nagendra Kumar | EC7190009 | 90 | 791 | 99.78 |
| 28 | MonikaG.K | EC1530164 | 90 | 791 | 99.78 |
| 29 | Sunil Kumar. V | EC1580438 | 96 | 787 | 99.76 |
| 30 | Jithin R | EC1470384 | 96 | 787 | 99.76 |

# ANALOG CIRCUITS

## CONTENTS



*For*

# *GATE, DRDO & IES*


*Managing Director*

*Prof. Y.V. Gopala Krishna Murthy*

# GATE SYLLABUS

## ANALOG CIRCUITS (ECE)

Small Signal Equivalent circuits of diodes, BJTs, MOSFETs and analog CMOS. Simple diode circuits, clipping, clamping, rectifier. Biasing and bias stability of transistor and FET amplifiers. Amplifiers: single-and multi-stage, differential and operational, feedback, and power. Frequency response of amplifiers. Simple op-amp circuits. Filters. Sinusoidal oscillators; criterion for oscillation; single-transistor and op-amp configurations. Function generators and wave-shaping circuits, 555 Timers. Power supplies.

## ANALOG CIRCUITS (EEE)

Characteristic of diodes, BJT, FET, SCR; amplifiers – biasing, equivalent circuit and frequency response; oscillators and feedback amplifiers; operational amplifiers - Characteristics and applications; simple active filters; VCO's timers.



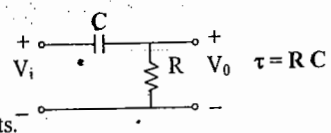
### 1.1: Wave Shaping Circuits

Wave shaping circuits are of two types

a) linear wave shaping circuits
b) non linear wave shaping circuits

### a. Linear Wave shaping circuits

The process by which the wave form of a non sinusoidal signal is altered by passing it through the linear network is called the linear wave shaping




$\tau = RC$

***High Pass Circuit***

This circuit is called the high pass filter because it passes the high frequency components and attenuates the low frequency components.

For low frequency, the reactance of the capacitance is large $X_C = \frac{1}{2\pi fC}$

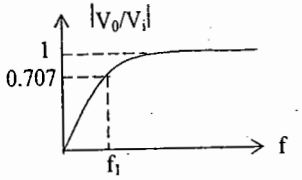
***(a) Sinusoidal input:***

$$\frac{V_0}{V_i} = \frac{R}{R + 1/j\omega C}$$

$$= \frac{1}{1 - j\frac{1}{\omega RC}}$$

$$\frac{V_0}{V_i} = \frac{1}{\sqrt{1 - j(f_l/f)}} \quad \text{Where } f_l = 1/2\pi RC$$

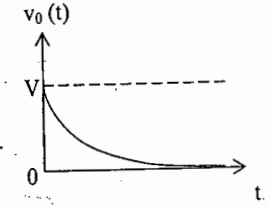
$$\left|\frac{V_0}{V_i}\right| = \frac{1}{\sqrt{1 + (f_l/f)^2}}, \quad \angle V_0 / V_i = -\tan^{-1}(-f_l/f) = \tan^{-1}(f_l/f)$$




***(b) Step input:*** $v_i(t) = v_c(t) + v_0(t)$, $v_i(t) = Vu(t)$

$= 1/C \int i\,dt + v_0(t)$

$v_0(t) = iR$, $1/RC \int v_0(t)\,dt + v_0(t) = Vu(t)$




It is a single time constant circuit and a first order equation is obtained

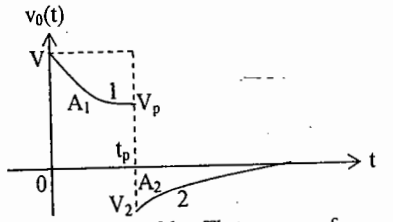
The general solution of any single time constant circuit can be written as

$v_0(t) = V_f + (V_i - V_f)\, e^{-t/\tau}$, here $V_f = 0$, $V_i = V$, $v_0(t) = Ve^{-t/\tau}$

***(c)Pulse input:*** $v_i(t) = V[u(t) - u(t - tp)]$

1) $v_0 = Ve^{-t/\tau}$, $V_p = V e^{-tp/\tau}$
2) $v_0 = V_2 e^{-(t-tp)/\tau}$, $V_2 = V_p - V$

$\tau$ large ⇒ slow response and
$\tau$ small ⇒ fast response




For a low time constant the peak-to-peak amplitude will be double. The process of converting pulses into spikes by means of a low time constant is called peaking.

In high pass RC circuit, the average level of the output is always zero. The area above the zero axis should be equal to the area below the zero axis, $A_1 = A_2$

### (d) Square wave input

For a non – symmetrical square wave $T_1 \neq T_2$, $T_1 + T_2 = T = 1/f$. The two extreme cases are

**case 1:** $\tau >> T_1$, $\tau >> T_2$. The I/P and O/P are shown below.

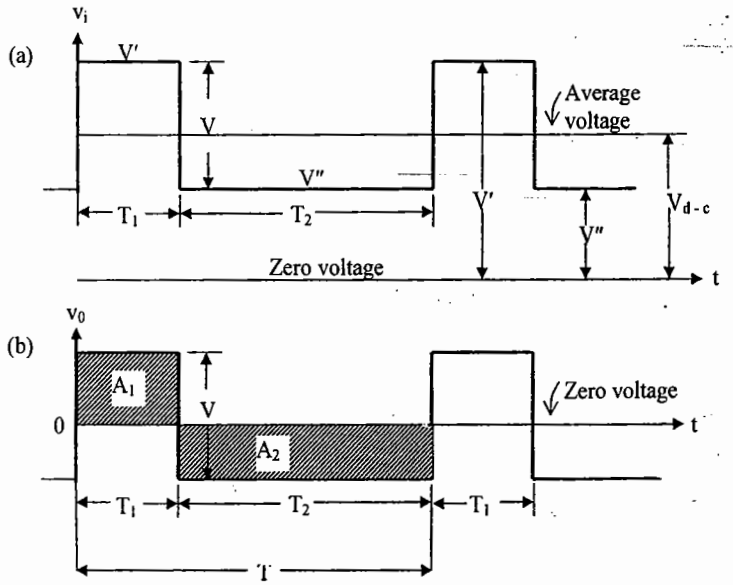



**Fig**: (a) Square wave input ;(b) Output voltage if the time constant is very large(compared with T).The d-c component $V_{d-c}$ of the output is always zero. Area $A_1$ equals area $A_2$.

**Case 2:** $\tau << T_1$, $\tau << T_2$. The response is shown below:

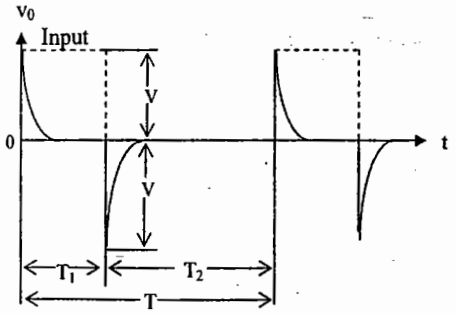



**Fig:** Peaking of a square wave resulting from a time constant small compared with T.



More generally the response to a square wave must have the appearance shown below:

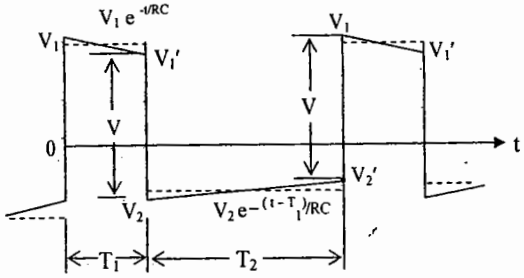
The four levels $V_1$, $V_1'$, $V_2$, $V_2'$ can be determined from

$V_1' = V_1 e^{-T_1/\tau}$ $V_1' - V_2 = V$

$V_2' = V_2 e^{-T_2/\tau}$ $V_1 - V_2' = V$

For symmetrical square wave:

$T_1 = T_2 = T/2$




$V_1 = -V_2$, $V_1' = V_2'$ and the response is shown below:

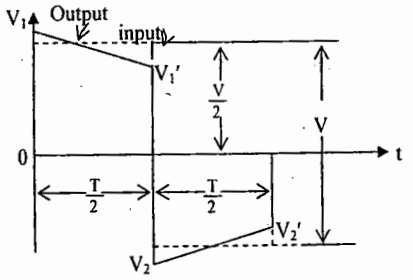



**Fig:** Linear tilt of a square wave when RC/T>> 1.

Percentage tilt 'P' is defined by

$$P = \frac{V_1 - V_1'}{V/2} \times 100 \approx \frac{T}{2\tau} \times 100\%$$

$$= \frac{\pi f_1}{f} \times 100\,\%$$

Where $f_1 = \frac{1}{2\pi\tau}$ and $f = 1/T$

### (e) Ramp input:

$v_i(t) = \alpha t\, u(t)$ and $v_0(t) = \alpha\tau(1 - e^{-t/\tau})$. are shown below,

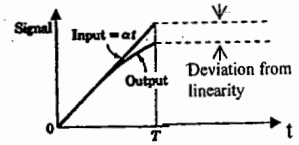



Fig (a)

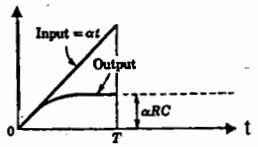


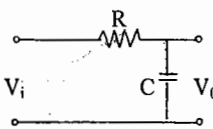

Fig (b)

Fig. (a) Response of a high pass RC circuit to a ramp voltage for RC / T>> 1;
(b) Response to a ramp voltage for RC / T << 1.

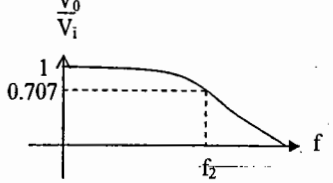
For $t << \tau$, as a measure of departure from linearity, transmission error, $e_t$ is defined as

$$e_t = \frac{v_i - v_o}{v_i}, \quad \text{At } t = T,\ e_t \approx T/(2\tau) = \pi f_1 T$$

**Low Pass Filter:**




This circuit allows the low frequency components and attenuates the high frequency components.




***(a) Sinusoidal input:***

$$\left|\frac{V_0}{V_i}\right| = \frac{1}{\sqrt{1 + (f/f_2)^2}}$$

$\angle V_0 / V_i = -\tan^{-1}(f / f_2)$, where $f_2 = 1/(2\pi RC)$

(b) ***Step input:***

$v_{i(t)} = Vu(t)$

$v_0(t) = V(1 - e^{-t/\tau})$

$t_r = 2.2\,\tau = 0.35 / f_2$

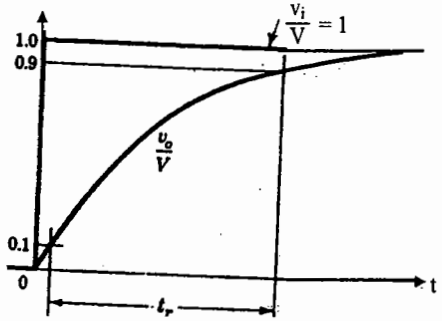



Fig. Step – voltage response of the low – pass RC circuit. The rise time $t_r$ is indicated.

**(C) Pulse input:**

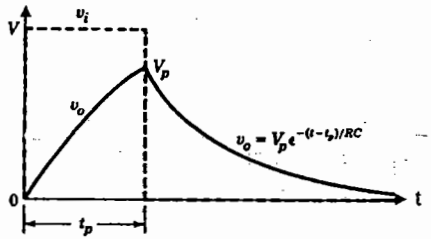



Fig. Pulse response of the low – pass RC circuits.

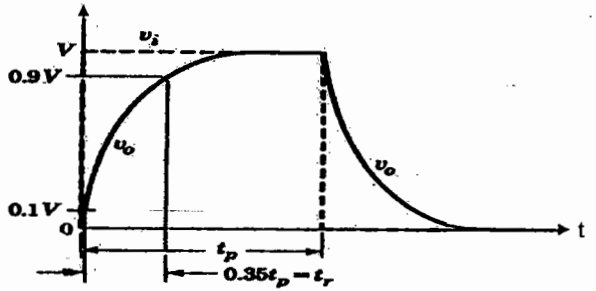



Fig. Pulse response for the case $f_2 = 1/t_p$



***(d) Square wave input:***

$v_{01} = V' + (V_1 - V')\,e^{-t/\tau}$

$v_{02} = V'' + (V_2 - V'')\,e^{-(t-T_1)/\tau}$

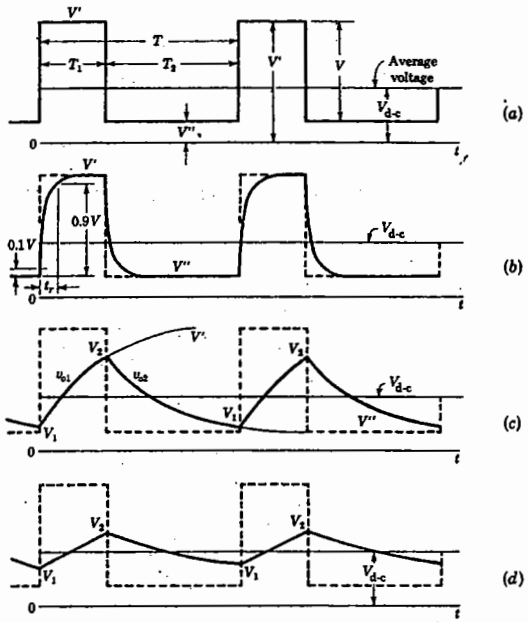
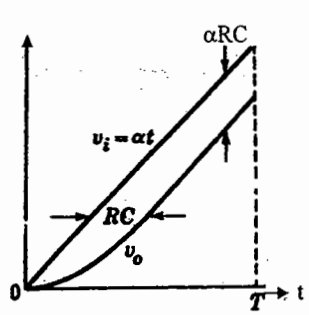



**Fig. 2-18** (a) Square-wave input; (b–d) output of the low-pass *RC* circuit. The time constant is smallest for (b) and largest for (d).

***(e) Ramp input:***



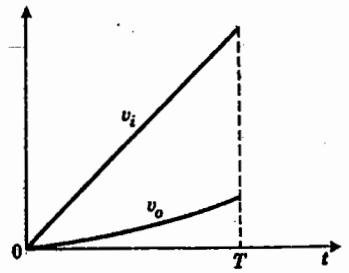




Fig. Response of a low – pass RC circuit to a ramp voltage
(a) $RC / T << 1$; (b) $RC / T >> 1$.

$v_0 = \alpha t - \alpha\tau\,(1 - e^{-t/\tau})$, $e_t \approx \tau / T = 1 / 2\pi f_2 T$

### *b. Non linear wave shaping circuits*

These devices are used for the purpose of switching.

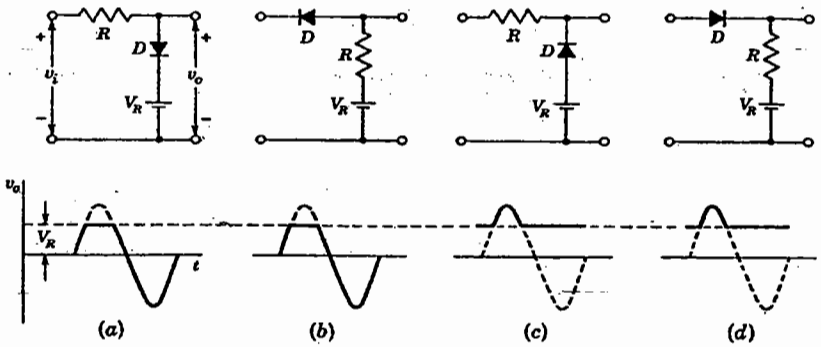
***CLIPPERS ( Limiters or amplitude selectors or slicers)***

There are a variety of diode networks called clippers that have the ability to "clip" off a portion of the input signal without distorting the remaining part of the alternating waveform. Depending on the orientation of the diode, the positive or negative region of the input signal is "clipped" off.

There are two general categories of clippers: series and parallel. The series configuration is defined as one where the diode is in series with the load, while the parallel variety has the diode in a branch parallel to the load.

There is no general procedure for analyzing clippers, but there are a few thoughts to be kept in mind as you work toward a solution.

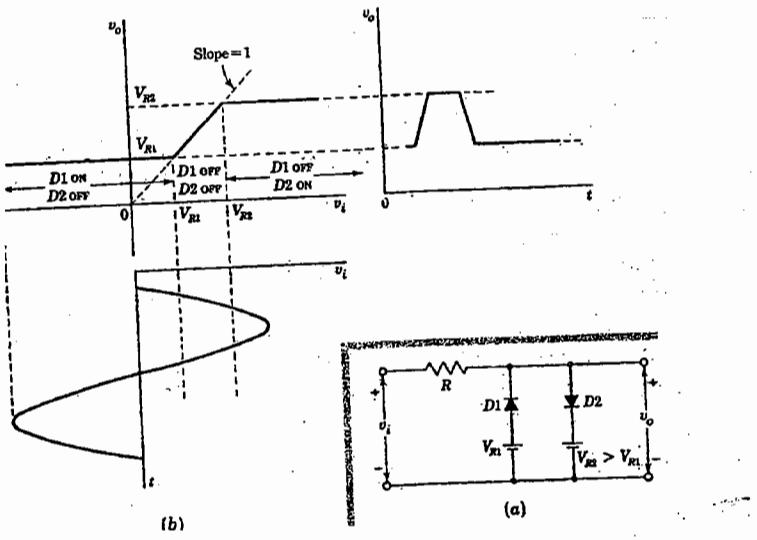
1. Make a mental sketch of the response of the network based on the direction of the diode and the applied voltage levels.
2. Determine the applied voltage (transition voltage) that will cause a change in state for the diode.
3. Be continually aware of the defined terminals and polarity of $V_0$.
4. It can be helpful to sketch the input signal above the output and determine the output.




It is reasonable to select $R = \sqrt{R_f R_r}$ .
The ratio $R_r / R_f$ may well serve as a figure of merit for diodes used in the present application.



**CLIPPING AT TWO INDEPENDENT LEVELS:**




This circuit is referred to as a slicer because the output contains a slice of the input between the two reference levels $V_{R1}$ and $V_{R2}$. The circuit is used as a means of converting a sinusoidal waveform into a square wave. In this application, to generate a symmetrical square wave, $V_{R1}$ and $V_{R2}$ are adjusted to be numerically equal but of opposite sign. The transfer characteristic passes through the origin under these conditions, and the waveform is clipped symmetrically top and bottom.

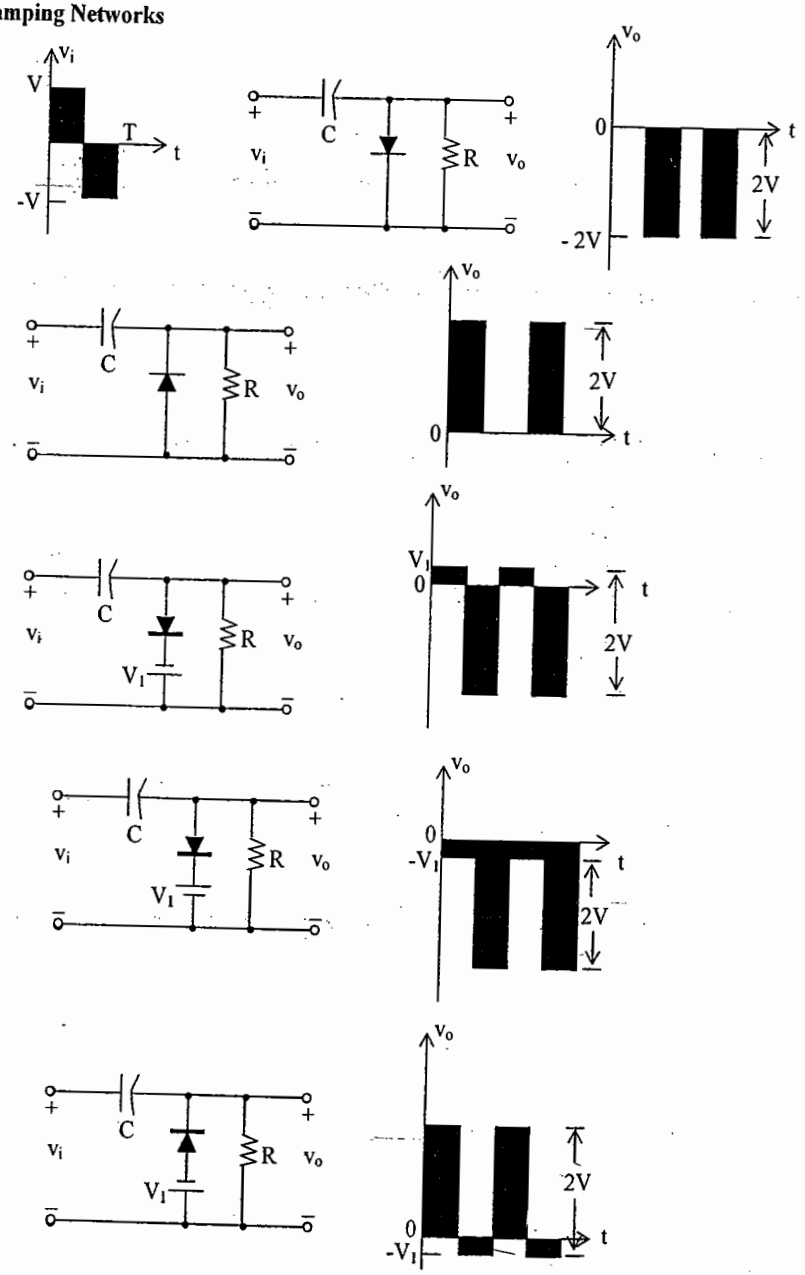
**CLAMPERS: -**

The clamping network is one that will "clamp" a signal to a different dc level. The network must have a capacitor, a diode, and a resistive element, but it can also employ an independent dc supply to introduce an additional shift. The magnitude of R and C must be chosen such that the time constant $\tau = RC$ is large enough to ensure that the voltage across the capacitors does not discharge significantly during the interval, the diode is non-conducting. The total swing of the output is equal to the total swing of the input signal. This fact is an excellent checking tool for the result obtained.

In general, the following steps may be helpful when analyzing clamping networks.

1. Start the analysis of clamping networks by considering that part of the input signal that will forward bias the diode.
2. During the period that the diode is in the "on" state, assume that the capacitor will charge up instantaneously to a voltage level determined by the network.
3. Assume that during the period when the diode is in the "off" state the capacitor will hold on to its established voltage levels.
4. Throughout the analysis maintain a continual awareness of the location and reference polarity for $V_0$ to ensure that the proper levels for $V_0$ are obtained.
5. Keep in mind the general rule that the total swing of the output must match the total swing of the input signal.

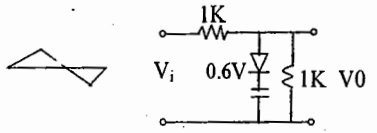
**Clamping Networks**



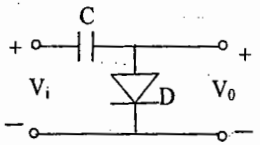



## OBJECTIVE QUESTIONS: SET - A

1. In figure the input $V_i$ is a 100 Hz triangular wave having a peak amplitude of 2 Volts and an average value of zero volt. Given that the diode is ideal, the average value of the output $V_0$ is .....




2. The circuit shown in acts as
   a) rectifier b) clamper
   c) clipper d ) comparator




3. The output waveform from an amplifier under pulse test has a rise time of 1μs. The upper 3dB frequency of the amplifier is

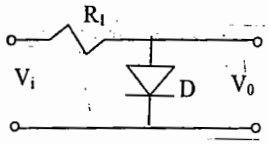
   a) 250 KHz b) 350 KHz c) 175 KHz d) none

4. An amplifier with a lower cut off frequency of 10 Hz is to be employed for amplification of square waves for the tilt on the output waveform not to exceed 2%.The lowest input frequency that can be amplified is

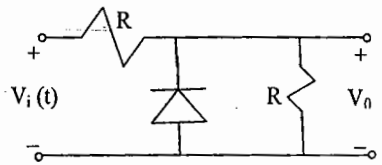
   a) 1.75 MHz b) 9.5 Hz c) 1.57 KHz d) 59.3 Hz

5. The circuit shown is to have an output voltage of 9V and an output current of approximately 1mA.If the input voltage is ±10V,the value of $R_1$ and the diode forward current, respectively are

   a) 1 KΩ, 6 mA
   b) 10 KΩ, 3 mA
   c) 1 KΩ, 9.3 mA
   d)10 KΩ, 1.5 mA




6. The average value of the output of the circuit for the input $V_i$ (t) = 10 Sinωt, is
   a) $10/\pi$
   b) $-10/\pi$
   c) $-5/\pi$
   d) $5/\pi$



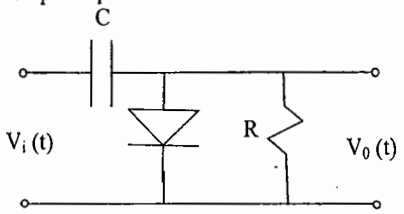
7 If input $V_i(t) = V_m \sin\omega t$, the output expression for the circuit shown is

a) $-V_m + V_m \sin\omega t$

b) $V_m - V_m \sin\omega t$

c) $-2V_m \sin\omega t$

d) $2V_m \sin\omega t$




8. In a clamping circuit the value of R across the diode is

a) The geometric mean of the forward and reverse resistance of that diode
b) The arithmetic mean of the forward and reverse resistance of that diode
c) The Harmonic mean of the forward and reverse resistance of that diode
d) The product of the forward and reverse resistance of that diode

9. In a clamping circuit the forward and reverse resistance of the diode used, Respectively, are 100 Ω and 120 KΩ. The value of R across the diode is

a) 60.05 KΩ b) 3.464 KΩ c) 12 MΩ d) 100 KΩ

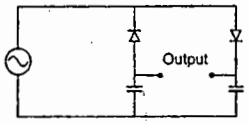
KEY: (1) 0 (2) b (3) b (4) c (5) c (6) d (7) a (8) a (9) b

## SET - B

01. The circuit shown in the figure is best described as

(A) bridge rectifier (B) ring modulator

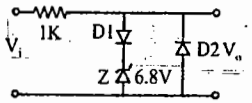
(C) frequency discriminator (D) voltage doubler




02. In the following limiter circuit, an input voltage $V_i = 101 \sin 100\pi t$ is applied. Assume that the diode drop is 0.7 V when it is forward biased. The zener breakdown voltage is 6.8 V. The maximum and minimum values of the output voltage respectively are

(A) 6.1 V, - 0.7 V (B) 0.7 V, - 7.5 V

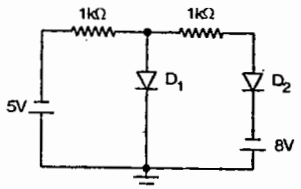
(C) 7.5 V, - 0.7 V (D) 7.5 V, - 7.5 V




03. Assuming that the diodes are ideal in figure, the current in diode $D_1$ is

(A) 8mA (B) 5 mA

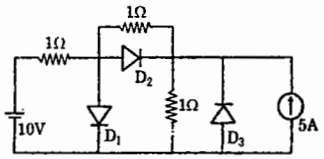
(C) 0 mA (D) – 3 mA




04. The states of the three ideal diodes of the circuit shown in figure are

(A) $D_1$ON, $D_2$ OFF, $D_3$ OFF (B) $D_1$OFF, $D_2$ ON, $D_3$ OFF

(C) $D_1$ON, $D_2$ OFF, $D_3$ ON (D) $D_1$OFF, $D_2$ ON, $D_3$ ON



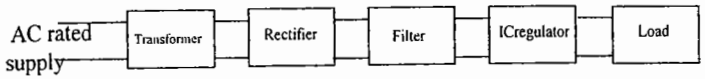

**KEY:** (1) D (2) C (3) C (4) A



## 1.2 RECTIFIERS AND POWER SUPPLIES:

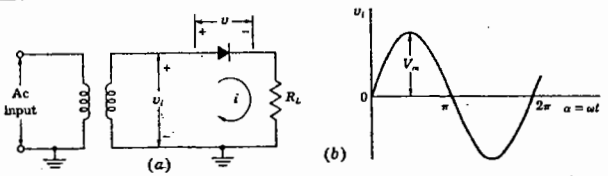
In a power supply, basically, starting with an AC voltage, a steady DC voltage is obtained by rectifying the AC voltage, then altering to a DC – level by filtering and finally regulating to obtain a desired fixed DC voltage.

### Block diagram of a typical power supply:



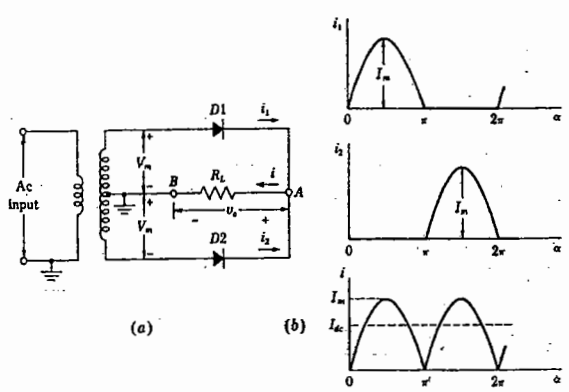

The AC voltage is connected to a transformer which steps that AC voltage down to the level for the desired DC output. A diode rectifier then provides a full-wave rectified voltage that is initially filtered by a simple capacitor filter to produce a DC voltage. This resulting DC voltage usually has some ripple or AC voltage variation. A regulator circuit can use this DC input to provide DC voltage that not only has much less ripple voltage but also remains almost the same DC value even if the input DC voltage varies some what, or the load connected to the output dc voltage changes. This voltage regulation is usually obtained by using one of a number of popular voltage regulator IC units.

### Half wave rectifier:

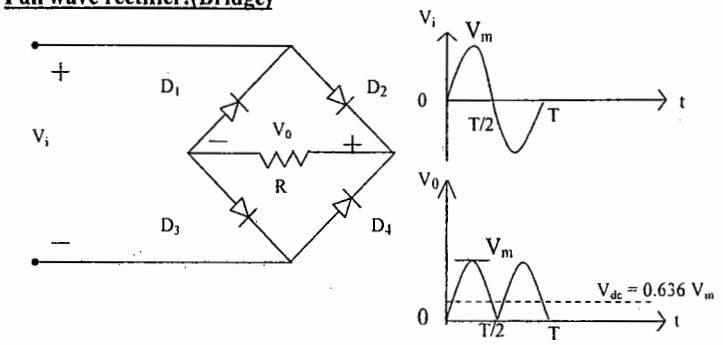



$v_i(t) = V_m \sin(\omega t)$

### Full wave rectifier: (CT transformer)

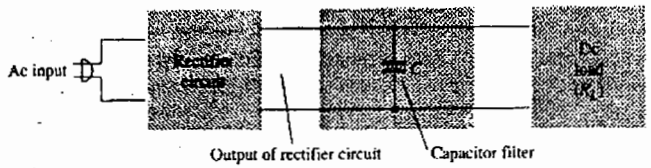


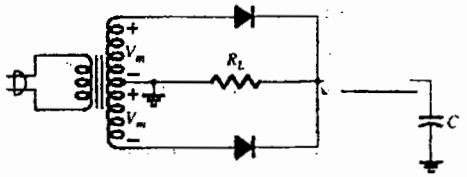
**Full wave rectifier:(Bridge)**

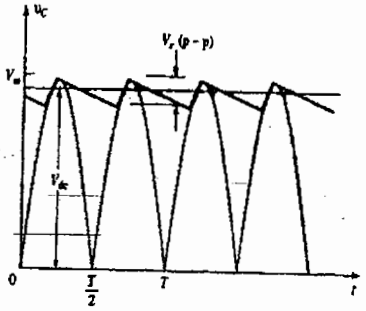



The output resulting from a rectifier is a pulsating DC voltage and not yet suitable as a battery replacement. A filter circuit is necessary to provide a steadier DC voltage.The filtered output has a DC value and some AC variation (ripple). A very popular filter circuit is the

**Capacitor filter circuit :**



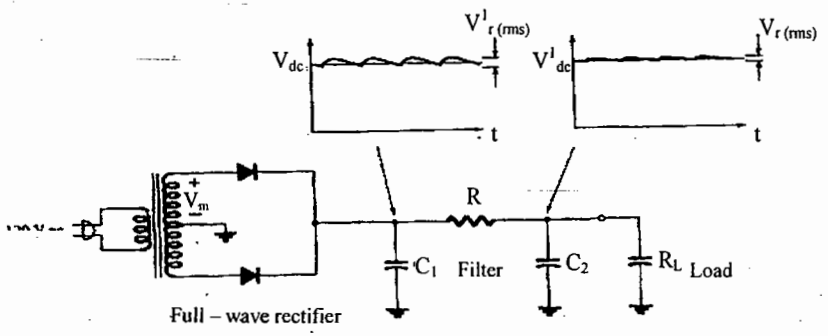




$V_{rms} = I_{dc} / (4\sqrt{3}\, f C)$

$r = V_{rms} / V_{dc} = 1 / (4\sqrt{3}\, f C R_L)$

The riple can be further reduced by using an additional RC section as shown below:

**Filter capaictor with additional RC filter section:**






| PARAMETER | HALF-WAVE | FULL-WAVE | BRIDGE |
|---|---|---|---|
| Ripple frequency($f_r$) | $f_s$ | $2 f_s$ | $2 f_s$ |
| P I V | $V_m$ | $2 V_m$ | $V_m$ |
| $I_m$ | $V_m / (R_f + R_L)$ | $V_m / (R_f + R_L)$ | $V_m / (2R_f + R_L)$ |
| Average current($I_{dc}$) | $I_m / \pi$ | $2 I_m / \pi$ | $2 I_m / \pi$ |
| R.M.S value($I_{rms}$) | $I_m / 2$ | $I_m / \sqrt{2}$ | $I_m / \sqrt{2}$ |
| D.C voltage($V_{d.c}$) | $V_m / \pi - I_{dc} R_f$ | $2 V_m / \pi - I_{dc} R_f$ | $2 V_m / \pi - 2 I_{dc} R_f$ |
| Form factor (F) | 1.57 | 1.11 | 1.11 |
| Ripple factor( r) | 1.21 | 0.482 | 0.482 |
| $P_{dc}$ | $I_{dc}^2 R_L$ | $I_{dc}^2 R_L$ | $I_{dc}^2 R_L$ |
| $P_i$ | $I_{rms}^2 (R_f + R_L)$ | $I_{rms}^2 (R_f + R_L)$ | $I_{rms}^2 (2R_f + R_L)$ |
| Efficiency($\eta_r$) | $\frac{40.5}{1 + (R_f / R_L)}$ % | $\frac{81.0}{1 + (R_f / R_L)}$ % | $\frac{81.0}{1 + (2R_f / R_L)}$ % |
| Regulation | $R_f / R_L \times 100$ % | $R_f / R_L \times 100$% | |

$f_s$ = a.c. input supply frequency, P I V ( Peak Inverse Voltage): The maximum voltage to which the diode is subjected in a rectifier circuit

$I_{dc} = \frac{1}{2\pi} \int_0^{2\pi} i \, d\alpha$ , $I_{rms} = \left( \frac{1}{2\pi} \int_0^{2\pi} i^2 \, d\alpha \right)^{0.5}$ , $V_{dc} = I_{dc} R_L$ , Form factor , $F = I_{rms} / I_{dc}$

$I'_{rms}$ = R M S value of the ac components of current $= (I_{rms}^2 - I_{dc}^2)^{0.5}$

Ripple factor , $r = I'_{rms} / I_{dc} = V'_{rms} / V_{dc} = \sqrt{F^2 - 1}$

$\eta_r$ = Efficiency of Rectification = $P_{dc} / P_i$, Regulation = $\frac{(V_{NL} - V_{FL})}{V_{FL}} \times 100$ %

## OBJECTIVES SET - A

1. In a series regulated power supply circuit, the voltage gain $A_v$ of the 'pass' transistor satisfies the condition:
   a. $A_v \to \infty$ b. $1 << A_r < \infty$ c. $A_r \approx 1$ d. $A_r << 1$

2. In rectifier circuits , the values of $V_{dc}$ , $V_{rms}$ , PIV rating of diode depends on the secondary voltage which is ultimately depends on _____
   a) primary voltage b) turns ratio c) both (a) & (b) d) none of the above

3. To get high regulated dc voltage which is greater than the rated voltage of a zener diode, zeners can be connected in _____
   a) series b) parallel c) none of the above

4 . For a given rectifier , calculate the value of ripple voltage if $V_{dc}$ = 10V ripple factor is 2%
   a) 0.2v b) 0.3V c) 0.4v d) none

5. A 10:1 transformer is use in half wave rectifier find no load voltage what is the PIV rating of diode used
   a) 23 b) $23\sqrt{2}$ c) $23\sqrt{5}$ d) none

6. If the ripple voltage in full wave rectifier is 25v at a load current of 60mA. What would be the value at a load current of 120mA.
   a) 100 V b) 25V c) 50V d) none

7. In a half wave rectifier , the load current flows for
   a) the complete cycle of the input signal
   b) only for positive half cycle of input signal
   c) less than half cycle of input signal
   d) more than half cycle but less than the complete cycle of input signal

8. In a half wave rectification if the input frequency is 50Hz, then the output has a frequency of
   a) 12.5Hz b) 25Hz c) 10Hz d) 50Hz

9. The disadvantage of half wave rectifier has a.c component _____ the d.c component
   a) components are expensive b) diodes must have a high power rating
   c) output is difficult to filter d) none

10. The out put of a half wave rectifier has a a.c component _____ the d.c component.
   a) equal to b) more than c) less than d) none



11. If the a.c input to a Half wave rectifier has an r.m.s value of $400/\sqrt{2}$ volts, then the diode PIV rating, is
   a) 400V b) $400/\sqrt{2}$ c) $400 \times \sqrt{2}$ d) $400 \times 3$

12. A full wave rectifier is _____ as effective as a half eave rectifier.
   a) twice b) thrice c) two and half times d) four times

13. In a full wave rectifier, the current in each of the diode flows for
   a) the complete cycle of input signal b) half cycle of input signal
   c) for zero time d) more than half cycle of input signal

14. In a full wave rectifier , if the input signal frequency is 50Hz, then output has a frequency of
   a) 100Hz b) 50Hz c) 25Hz d) 200Hz

15. The bridge rectifier is preferable to an ordinary two – diode full wave rectifier because
   a) it uses four diodes b) transformer has center – tap
   c) needs much smaller transformer for the same output d) it has higher safety factor

16. In full wave rectification, transformer is _____
   a) essential b) center tapped c) both (a) & (b) d) none

17. The a.c. component in the output of a full wave rectifier is ..... the d.c component
   a) equal to b) more than c) less than d) none

18. The PIV of each diode in a bridge circuit is _____ that of equivalent center - tap circuit
   a) equal to b) half c) greater than d) none

19. The primary function of a center – tapped transformer in a power supply is to _____
   a) step up the voltage b) step down the voltage
   c) causes the diodes conduct alternatively d) none

20. For the same secondary voltage, the output voltage from a center – tap circuit is _____ than that of bridge circuit
   a) twice b) thrice c) four times d) one half

21. If PIV rating of a diode is exceeded, the diode _____
   a) stops conduction b) is destroyed
   c) conducts heavily in the forward direction d) none

22. The rectifier which of power supply is a measure of
   a) half wave rectifier b) full wave rectifier
   c) voltage doubles circuit d) none

23. The ripple factor of power supply is a measure of
a) its filter efficiency b) diode rating
c) its voltage regulation d) purity of power output

24. In a half wave rectifier, the peak value of the a.c voltage across the secondary of the transformer is $20\sqrt{2}$ if no filter circuit is used the max. d.c voltage across the load will be
a) 28.28V b) 25V c) 14.14V d) 9V

25. In a full wave rectifier $V_m$ is the peak voltage between the center tap and one of the secondary the max voltage across the reverse biased diode is _____
a) $V_m$ b) ½ $V_m$ c) $2V_m$ d) $4V_m$

26. The most widely used rectifier circuit is
a) HWR b) center – tap circuit c) bridge circuit d) none

27. A crystal diode can be used as a rectifier because it offers
a) low resistance in both directions
b) high resistance in one direction and low resistance in the other direction
c) high resistance in both direction
d) none

28. A center tap circuit utilizes _____ secondary voltage for full wave rectification
a) full b) only half of c) one fourth of d) none

29. The bridge rectifier provides 50mA current at 150V. the transformer voltage specification is
a) 220V: 167V b) 120 V: 150V c) 220V: 236V d) 120V:110V

30. The bridge rectifier provides 50 mA current at 150V. the average current and PIV of each diode, respectively are
a) 79mA, 167V b) 25mA, 236V c) 79mA, 167V d) 25mA, 120V

31. If the ripple factor of the output wave of a rectifier us low, it means that
a) output voltage will have less ripple b) output voltage will be low
c) filter circuits may not be required d) none

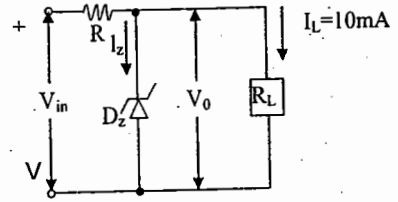
**Key :** (01).C (02).C (03).B (04).A (05).B (06).C (07).B (08).D
(09).C (10).B (11).A (12).A (13).B (14).A (15).C (16).C (17).C
(18).B (19).B (20).D (21).B (22).B (23).D (24).D (25).C (26).C
(27).B (28).B (29).A (30).B (31).A



**SET - B**

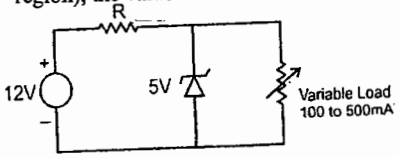
01. A dc power supply has a no – load voltage of 30 V, and a full – load voltage of 25 V at a full – load current of 1 A. Its output resistance and load regulation, respectively, are
(A) 5 Ω and 20% (B) 25Ω and 20%
(C) 5 Ω and 16.7% (D) 25Ω and16.7%

02. A zener diode regulator in the figure is to be designed to meet the specifications: $I_L = 10$ mA, $V_0 = 10$ V and $V_{in}$ varies from 30 V to 50V. The zener diode has $V_z = 10$V and $I_{ZK}$ (knee current) = 1 mA. For satisfactory operation




(A) $R \le 1800\ \Omega$
(B) $2000\ \Omega \le R \le 2200\ \Omega$
(C) $3700\ \Omega \le R \le 4000\ \Omega$
(D) $R > 4000\ \Omega$

03. In the voltage regulator shown in the figure, the load current can vary from 100 mA. Assuming that the Zener diode is ideal (i.e., the Zener knee current is negligibly small and Zener resistance is zero in the breakdown region), the value of R is




(A) 7 Ω (B) 70 Ω
(C) 70/3 Ω (D) 14 Ω

04. In a full – wave rectifier using two ideal diodes, $V_{dc}$ and $V_m$ are the dc and peak values of the voltage respectively across a resistice load. If PIV is the peak inverse voltage of the diode, then the appropriate relationships for this rectifier are

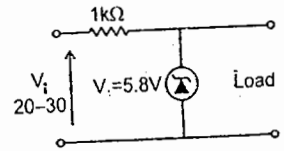
(A) $V_{dc} = \frac{V_m}{\pi}$, PIV = 2 $V_m$

(B) $V_{dc} = 2\frac{V_m}{\pi}$, PIV = 2 $V_m$

(C) $V_{dc} = 2\frac{V_m}{\pi}$, PIV = $V_m$

(D) $V_{dc} = \frac{V_m}{\pi}$, PIV = $V_m$

05. The zener diode in the regulator circuit shown in the figure has a zener voltage of 5.8 volts and a zener knee current of 0.5 mA. The maximum load current drawn from this circuit ensuring proper functioning over the input voltage range between 20 and 30 volts, is

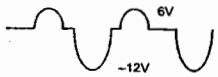



(A) 23.7 mA (B) 14.2 mA
(C) 13.7 mA (D) 24.2 mA

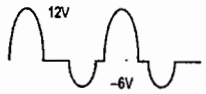
06. For the circuit shown below, assume that the zener diode is ideal with a breakdown voltage of 6 volts. The waveform observed across R is

(A)

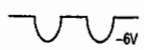

(B)




(C)

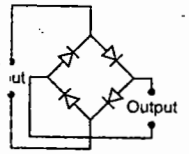



(D)

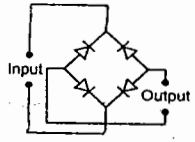



07. The correct full rectifier circuit is

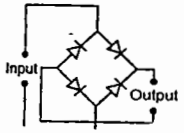
(A)



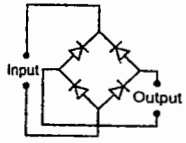

(B)



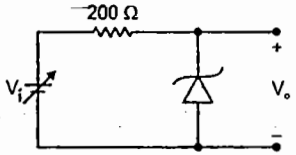

(C)




(D)




08. For the zener diode shown in the figure, the zener voltage at knee is 7 V, the knee current is negligible and the zener dynamic resistance is 10 Ω. If the input voltage ($V_i$) range is from 10 to 16 V, the output voltage ($V_0$) ranges from




(A) 7.00 to 7.29 V

(B) 7.14 to 7.29 V

(C) 7.14 to 7.43 V

(D) 7.29 to 7.43 V

KEY :

| | | |
|---|---|---|
| (1) B | (2) A | (3) D |
| (4) B | (5) A | (6) B |
| (7) C | (8) C | |



## DC BIASING-BJTs

The analysis or design of a transistor amplifier requires knowledge of both the dc and ac response of the system. Too often it is assumed that the transistor is a magical device that can raise the level of the applied ac input without the assistance of an external energy source. In actuality, the improved output ac power level is the result of a transfer of energy from the applied dc supplies. The analysis or design of any electronic amplifier, therefore, has two components; the dc portion and the ac portion.

- Depending on the biasing of the junciton there are four modes in which a transistor can operate.

| | $J_E$ | $J_C$ |
|---|---|---|
| i) | FB | FB ----Saturation mode |
| ii) | FB | RB--- Active mode |
| iii) | RB | FB ---- Inverted mode |
| iv) | RB | RB --- Cut off mode. |

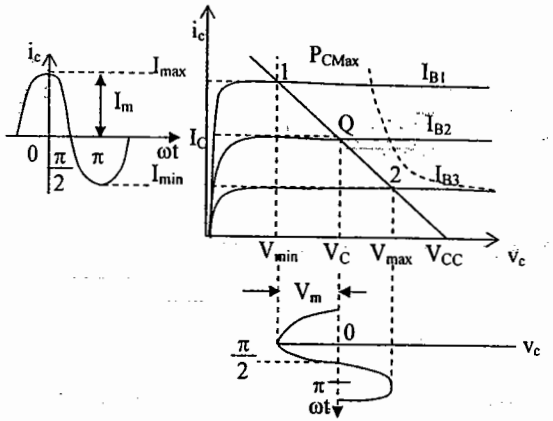
- . A Transistor can be operated as a switch when operated in saturation and cut off modes.
- A Transistor can be used as an amplifier in active mode.
- The transistor dissipates maximum power when it is operated in active mode.
- Power dissipation in the transistor is given by $P_D=I_CV_{CE}$
- Dissipation in the transistor is minimum in saturation and cut off modes.
- In active mode the collector current depends on base current and is independent of collector emitter voltage.
- Inverted mode is not used since the current gain is very low

For the BJT to be biased in its linear or active operating region the following must be true:

1. The base – emitter junction must be forward-biased with a resulting forward bias voltage of about 0.6 to 0.7V.
2. The base – collector junction must be reverse-biased, with the reverse-bias voltage being any value within the maximum limits of the device.

***OPERATING POINT→***

The term biasing appearing in the title of this chapter is an all inclusive term for the application of dc voltages to establish a fixed level of current and voltage. For transistor amplifiers the resulting dc current and voltage establish an operating point on the characteristics that define the region that will be employed for amplification of the applied signal. Since the operating point is a fixed point on the characteristics it is also called the quiescent point (abbreviated Q- point). By definition, quiescent means quiet, still, inactive. The following figure shows a general output device characteristics. The biasing circuit can be designed to set the device operation at Q ($V_C$, $I_C$) within the active region. The maximum ratings are indicated on the characteristics by a horizontal line for the maximum collector current $I_{c\ max}$ and a vertical line at the maximum collector-to-emitter voltage $V_{CE\ max}$. The maximum power constraint is defined by the curve $P_{Cmax}$.




## BIAS STABILIZATION

Temperature causes the device parameters such as the transistor current gain ($\beta_{ac}$) and the transistor leakage current ($I_{CEO}$) to change. Higher temperatures result in increased leakage currents in the device, thereby changing the operating condition set by the biasing network. The result is that the network design must also provide a degree of temperature stability so that temperature changes result in minimum changes in the operating point. This maintenance of the operating point can be specified by a stability factor, S, which indicates the degree of change in operating point due to temperature variation.

Thus the stability of a system is a measure of the sensitivity of a network to variations in its parameters. The collector current $I_c$ is sensitive to each of the following parameters.

$\beta$: increases with increase in temperature

$V_{BE}$: decreases about 7.5 mV per degree Celsius (°C) increase in temperature.

$I_{CO}$ (reverse saturation current) : doubles in value for every 10°C increase in temperature.

Any or all of these factors can cause the bias point to drift from the designed point of operation.

$$I_C = f(I_{CO}, V_{BE}, \beta)$$

$$\Delta I_C = \frac{\partial I_C}{\partial I_{C0}} \Delta I_{CO} + \frac{\partial I_C}{\partial V_{BE}} \Delta V_{BE} + \frac{\partial I_C}{\partial \beta} \Delta \beta$$

$$\Delta I_C = S \Delta I_{CO} + S' V_{BE} + S'' \Delta\beta$$

$S, S', S''$ are stability factors where

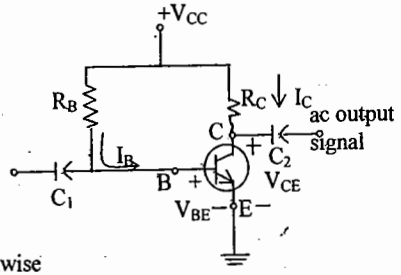
$$S = \frac{\partial I_C}{\partial I_{C0}} \Big|_{V_{BE}, \beta \text{const}}$$

$$S = \frac{\partial I_C}{\partial V_{BE}} \Big|_{I_{CO}, \beta \text{const}}$$

$$S = \frac{\partial I_C}{\partial \beta} \Big|_{I_{CO}, V_{BE} \text{const}}$$



*FIXED BIAS CIRCUIT→*




The fixed bias circuit provides a relatively straight forwad and simple introduction to transistor dc bias analysis.

**Base-Emitter Loop:** consider the base emitter circuit loop, writing Kirchoff's voltage equation in the clockwise direction for the loop, we obtain.

$$+V_{CC} - I_B R_B - V_{BE} = 0$$

$$\therefore I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

Since the supply voltage $V_{CC}$ and the base-emitter voltage $V_{BE}$ are constants, the selection of $R_B$, sets the levels of base current for the operating point.

**Collector-Emitter Loop:** $I_C = \beta I_B$

Since the base current is controlled by the level of $R_B$ and $I_C$ is related to $I_B$ by a constant $\beta$ the magnitude of $I_C$ is not a function of the resistance $R_C$. However, the level of $R_C$ will determine the magnitude of $V_{CE}$. Applying KVL in the clockwise direction around the closed loop

$V_{CE} + I_C R_C - V_{CC} = 0$ and $V_{CE} = V_{CC} - I_C R_C$

But $V_{CE} = V_C - V_E = V_C$ and $V_{BE} = V_B - V_E = V_B$ Since $V_E = 0V$

**Transistor saturation:** For a transistor operating in the saturation region the current is a maximum value for the particular design. The highest saturation level is defined by the maximum collector current. To know the approximate maximum collector current for a design, simply insert a short-circuit equivalent between collector and emitter of the transistor and calculate the resulting collector current. For the fixed bias, the short circuit has been applied, causing the voltage across $R_C$ to be the applied voltage $V_{CC}$.

$$I_{C\,sat} = \frac{V_{CC}}{R_C}$$

Here $I_B$ is fixed because the biasing voltage $V_{CC}$ and base resistance $R_B$ are constant. As the temperature increases $I_{CO}$ increases hence $I_C$ increases. As $I_C$ increases temperature increases so again $I_{CO}$ increases. This cumulative process leads to thermal run away because here $I_B$ is constant

$I_C = \beta I_B + (1+\beta) I_{CO}$ Stability factor, $S = \frac{\partial I_C}{\partial I_{CO}}$

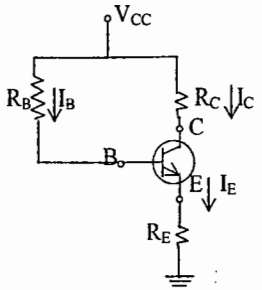
Since $I_B$ is constant, $\frac{\partial I_B}{\partial I_C} = 0$

$$\therefore S = \frac{1+\beta}{1 - \beta \frac{\partial I_B}{\partial I_C}} = 1 + \beta$$

From the above equation we can conclude that for a small change occurring in $I_{CO}$ makes a large change in $I_C$. So, this circuit gives less stability and not commonly used.

*FIXED BIAS CIRCUIT WITH EMITTER RESISTOR →*

**Base Emitter loop:**




Writing Kirchoff's voltage law in the clockwise direction

$$+V_{CC} - I_B R_B - V_{BE} - I_E R_E = 0$$

But $I_E = (1+\beta) I_B$

$$\therefore V_{CC} - I_B R_B - V_{BE} - (\beta+1) I_B R_E = 0$$

$$\therefore I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1) R_E}$$

$$I_C = \beta I_B = \frac{\beta [V_{CC} - V_{BE}]}{R_B + (1 + \beta) R_E}$$

Since $\beta >> 1$ and $V_{BE}$ is very small,

$$I_C \approx \frac{V_{CC}}{R_E + \frac{R_B}{\beta}}$$

**Collector-Emitter Loop:**

Writing KVL in the clockwise direction,

$$I_E R_E + V_{CE} + I_C R_C - V_{CC} = 0$$

Substituting $I_E \cong I_C$

$$V_{CE} = V_{CC} - I_C (R_C + R_E)$$

Again consider the Base-emitter loop,

$$I_B = \frac{V_{CC} - V_{BE} - I_C R_E}{R_B + R_E}$$

$$\frac{\partial I_B}{\partial I_C} = \frac{-R_E}{R_B + R_E}$$

Stability factor $S = \dfrac{1+\beta}{1 - \beta \dfrac{\partial I_B}{\partial I_C}}$ $S = \dfrac{1+\beta}{1 + \dfrac{\beta R_E}{R_E + R_B}}$

An increase in $I_C$ due to an increase in $I_{CO}$ will cause the voltage $V_E = I_E R_E \cong I_C R_E$ to increase. The result is a drop in the level of $I_B$. A drop in $I_B$ will have the effect of reducing the level of $I_C$ through transistor action and thereby offset the tendency of $I_C$ to increase due to an increase in temperature. In total, therefore, the configuration is such that there is a reaction to an increase in $I_C$ that will tend to oppose the change in bias conditions.
To decrease the stability factor we have to increase $R_E$ value, but this

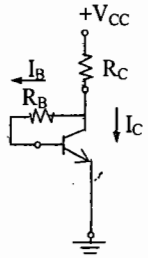
- decreases the gain of the amplifier
- increases voltage drop across $R_E$

The first draw back can be avoided by connecting a by pass capacitor across $R_E$ but the second one cannot be avoided. Hence this circuit is not used.



*COLLECTOR TO BASE BIASING CIRCUIT (Self Bias)*

**Base-Emitter loop:** Applying KVL




$$V_{CC} - (I_B + I_C) R_C - I_B R_B - V_{BE} = 0$$

$$V_{CC} - I_B(R_C + R_B) - I_C R_C - V_{BE} = 0$$

$$I_B = \frac{V_{CC} - I_C R_C - V_{BE}}{R_B + R_C}$$

**Collector Emitter loop :** Applying KVL $V_{CC} - (I_C + I_B) R_C - V_{CE} = 0$

Neglecting $I_B$, $V_{CC} - V_{CE} - I_C R_C = 0$

$$V_{CE} = V_{CC} - I_C R_C$$

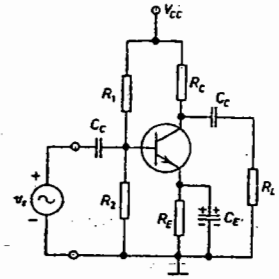
Stabilizing factor = $S = \dfrac{1+\beta}{1 - \beta \dfrac{\partial I_B}{\partial I_C}}$ $\dfrac{\partial I_B}{\partial I_C} = \dfrac{-R_C}{R_B + R_C}$ $S = \dfrac{1+\beta}{1 + \dfrac{\beta R_C}{R_B + R_C}} \cong 1$ for $R_C >> R_B$

$R_B$ is the feedback resistor and eliminating the feedback is difficult. So this method is rarely used.

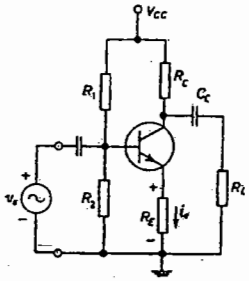
This feedback configuration operates in much the same way as the emitter-bias configuration when it comes to levels of stability. If $I_C$ should increase due to an increase in temperature, the level of V across $R_C$ will increase and the level of $I_B$ will decrease. The result is a stabilizing effect as described for the emitter-bias configuration.

*SELF BIAS CIRCUIT →*

This Voltage divider biasing circuit is the most widely used circuit.




Voltage Divider biasing with bypass capacitor

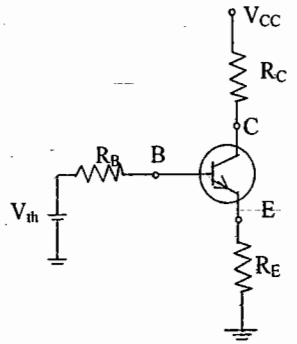


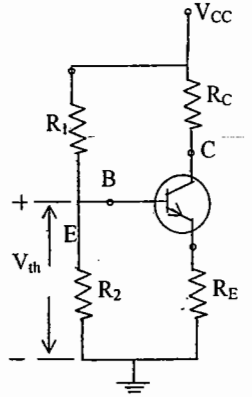

Voltage Divider biasing without bypass capacitor

Applying Thevenin's Theorem at the input side,

$$V_{th} = V_{CC} \frac{R_2}{R_1 + R_2}$$

$$R_B = \frac{R_1 R_2}{R_1 + R_2}$$



Applying KVL to input, $-V_{th} + I_B R_B + V_{BE} + I_E R_E = 0$

$V_{th} = I_B R_B + V_{BE} + R_E (I_C + I_B)$

$$I_B = \frac{V_{th} - V_{BE} - R_E I_C}{R_B + R_E}$$

$I_C = \beta I_B$

Applying KVL to output,

$V_{CC} - I_C R_C - V_{CE} - (I_C + I_B) R_E = 0$

$V_{CE} = V_{CC} - I_B R_E - I_C (R_C + R_E)$

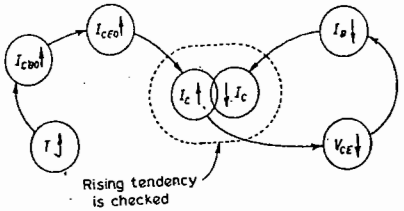
Neglecting $V_{BE}$, $I_C \cong \frac{\beta V_{th}}{R_B + (1+\beta) R_E}$ Since $\beta >> 1$ $I_C = \frac{V_{th}}{\frac{R_B}{\beta} + R_E}$

Stability factor, $S = \frac{1+\beta}{1 - \beta \frac{\partial I_B}{\partial I_C}}$ $\frac{\partial I_B}{\partial I_C} = \frac{-R_E}{R_B + R_E}$

$$\frac{\partial I_B}{\partial I_C} = \frac{-R_E}{R_B + R_E}$$

$$S = \frac{1+\beta}{1 + \frac{\beta R_E}{R_B + R_E}} \cong 1 \text{ for } R_B << R_E$$

Negative feedback can be eliminated by connecting a by pass capacitor across $R_E$. The most stable of the configurations is the voltage divider bias network. If the condition $\beta R_E >> 10 R_2$ is satisfied, the voltage $V_B$ will remain fairly constant for changing levels of $I_C$. The base to emitter voltage of the configuration is determined by $V_{BE} = V_B - V_E$. If $I_C$ should increase, $V_E$ will increase and for a constant $V_B$ the voltage $V_{BE}$ will drop. A drop in $V_{BE}$ will establish a lower level of $I_B$ which will try to offset the increased level of $I_C$.




## COMPENSATION TECHNIQUES

The compensation technique is used only to compensate the temperature parameters and not to fix the operating point in active region. The operating point is fixed by stabilization technique by using biasing resistors. So, the compensation technique is applicable only after the stabilization. With compensation technique we can compensate temperature parameter exactly.

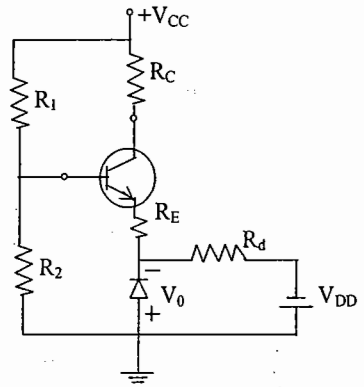
There are four types of compensation techniques available.

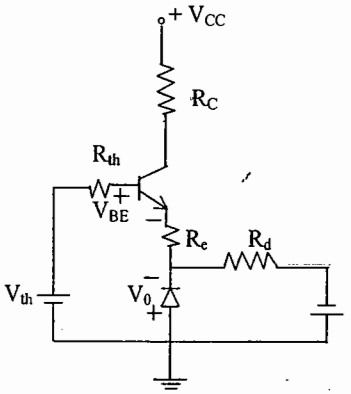
i) Diode compensation for $V_{BE}$ ii) Diode compensation for $I_{CO}$

iii) Thermistor compensation iv) Sensistor compensation



### *DIODE COMPENSATION FOR $V_{BE}$ →*




The variation in $V_{BE}$ can be cancelled by connecting the diode in series with emitter such that the voltage across diode is in opposite direction to $V_{BE}$. Here the diode and transistor are made with same material to get the same temperature effect in both the devices.

Apply KVL to Thevenin's equivalent circuit,

$V_{th} - I_B R_{th} - V_{BE} - I_E R_E + V_0 = 0$

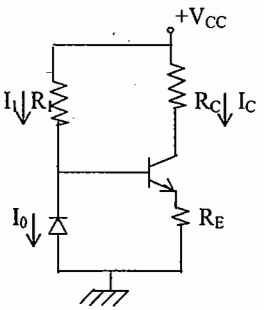
Since $V_0 = V_{BE}$

$$V_{th} - R_{th} I_B - R_E (\beta I_B + I_B) = 0$$

$V_{BE} = V_0$ because any change in $V_{BE}$ due to temperature the same change occurs in $V_0$. So, the collector current is independent of $V_{BE}$.

### *DIODE COMPENSATION FOR $I_{CO}$ →*

If the diode and transistor are made of same material then the reverse saturation current $I_0$ of the diode will increase with temperature at the same rate as the transistor reverse saturation current $I_{CO}$




$I_C = \beta I_B + (1+\beta) I_{CO}$

$I_B = I_1 - I_0$

$\therefore I_C = \beta (I_1 - I_0) + (1+\beta) I_{CO}$.

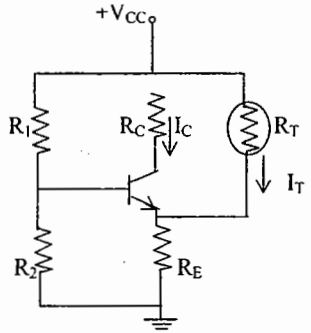
since $\beta >> 1$

$I_C = \beta (I_1 - I_0) + \beta I_{CO}$

$I_C = \beta I_1 - \beta (I_0 - I_{CO})$

$I_C = \beta I_1$ Since $I_0 = I_{CO}$

*THERMISTOR COMPENSATION →*




Thermistor is a temperature sensitive device having a negative temperature coefficient (ie) its resistance decreases with increase in temperature.

So,

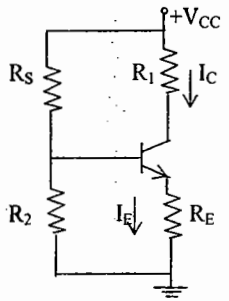
$T\uparrow \rightarrow R_T\downarrow \rightarrow I_T\uparrow \rightarrow I_E R_E\uparrow \rightarrow I_B\downarrow \rightarrow I_C\downarrow$

$\downarrow$

$I_C\uparrow$

Thermistors are used to minimize the increase in $I_C$ due to change in temperature.

*SENSISTOR COMPENSATION →*

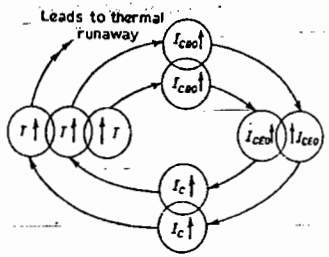



Sensistor is a heavily doped semiconductor device having positive temperature coefficient, (ie) its resistance increases with temperature.

**THERMAL STABILITY**

Thermal stability is the condition to avoid the thermal runaway.

The increase in $I_C$ due to increase in temperature gives more power dissipation in the collector junction. Due to the power dissipation in the collector junction again temperature increases. So, $I_C$ again increases. This cumulative process gives more heat at collector junction and spoils the transistor. This process is called Thermal Runway.




*CONDITION FOR THERMAL STABILITY →*

The steady state temperature rise at collector junction is proportional to power dissipation at the junction.

$$(T_j - T_A) \alpha P_D$$

where $T_j$ – junction temperature

$T_A$ – Ambient temperature



$$T_j - T_A = \theta P_D$$

Where $\theta$ thermal resistance °C/watt

To get the change in power dissipation with respect to junction temperature, partially differentiate with respect to $T_j$

$$1 - 0 = \theta \frac{\partial P_D}{\partial T_j}$$

$$\frac{\partial P_D}{\partial T_j} = \frac{1}{\theta}$$

Condition for thermal stability is the rate at which heat is generated at collector junction should be less than the rate at which heat dissipated.

$$\text{(ie)} \quad \frac{\partial P_C}{\partial T_j} < \frac{\partial P_D}{\partial T_j}$$

$$\Rightarrow \quad \frac{\partial P_C}{\partial T_j} < \frac{1}{\theta}$$

This is the condition to avoid thermal runaway

$$\frac{\partial P_C}{\partial T_j} = \left(\frac{\partial P_C}{\partial I_C}\right)\left(\frac{\partial I_C}{\partial I_{C0}}\right)\left(\frac{\partial I_{C0}}{\partial T_j}\right) < \frac{1}{\theta}$$

$\frac{\partial I_C}{\partial I_{C0}}$ → Stability factor

$\frac{\partial I_{C0}}{\partial T_j}$ → 7 % per $^0$C $= 0.07\ I_{C0}$

**OBJECTIVE QUESTIONS: SET A**

1. Thermal runaway in a transistor biased in the active region is due to

   a) heating of the transistor
   b) changes in $\beta$ which increases with temperature
   c) base emitter voltage $V_{BE}$ which decreases with rise in temperature
   d) change in reverse collector saturation current due to rise in temperature.

2. To obtain a fixed bias in CE configuration, a battery of 2V is used in the base with a series resistor $R_B$ across the base emitter junction; given $\beta = 100$ and $V_{BE} = 0.6$ Volt, to obtain $I_C = 2$mA, the value of $R_B$ is given by

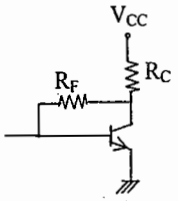
   a) 700 ohms b) 7 K ohms c) 70 K ohms d) 130 K ohms

3. In the self biasing scheme or collector - to - base biasing circuit ( $R_F$ across collector to base) of a BJT, $S_I$ tends to unity by

   a) increasing $R_F$ b) decreasing $R_C$
   c) decreasing $R_F$ and increasing $R_C$ d) increasing $R_F$ and decreasing $R_C$

   Note: $R_C$ is collector load resistor.

4. In the circuit shown $V_{CC}$ =10, $R_C$ = 2.7 K, $R_F$ = 200 K, β = 99, $V_{EB}$ = 0.6. The operating point $V_C$, $I_C$ are given by




a) 4.6 V and 1.98 mA
b) 4.7 V and 2 mA
c) 5.4 V and 1.56 mA
d) 4.2 V and 2.1 mA

5. In the potential divider bias (with $R_{B1}$ and $R_{B2}$) to obtain base current, $R_B$ is the equivalent base resistor and $R_E$ the emitter resistor.

a) $R_B >> R_E$ improves $S_I$ b) $R_B >> R_E$ improves $S_\beta$
c) $R_B << R_E$ improves both $S_I$ and $S_\beta$ d) $R_B$ has no effect on the stabilization factors

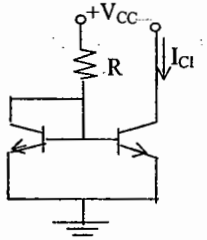
6. In regard to the operating point of a transistor in the active region, and its stabilisation, following four statements are made:.

1. $I_{CO}$ doubles for every 10°C rise in temperature.
2. $V_{BE}$ increases with temperature
3. Potential divider bias along with $R_E$ stabilizes against variations in $I_{CO}$ but not in $\beta_0$
4. For good stabilization, $R_B << R_E$, where $R_B$ is the equivalent base resistor of the potential divider resistors. Of these, the true statements are

a) only 1,2 b) only 2,3 c) only 3,4 d) only 4, 1

7. Circuit shows current mirror biasing for IC's. Given $V_{CC}$ = 10 volts, $I_{CI}$ = 1 mA and $V_{BE}$ = 0.7 volt, the value of R is given by

a) 10 K Ω
b) 9.3 K Ω
c) 5 KΩ
d) 4.65 K Ω




8. In a CE amplifier, the effect of an unbypassed $R_E$ is to increase the input resistance. This happens because

1. The system tends towards an ideal CVS
2. Both input and output currents flow through $R_E$
3. The fed back quantity is a voltage
4. The fed back quantity is a current.

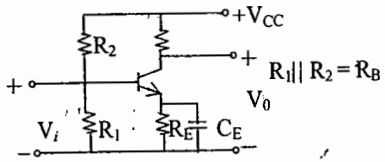
Of the above four statements the true statements are

a) only 1,2 b) only 3,4 c) only 2,3 d) only 1,4

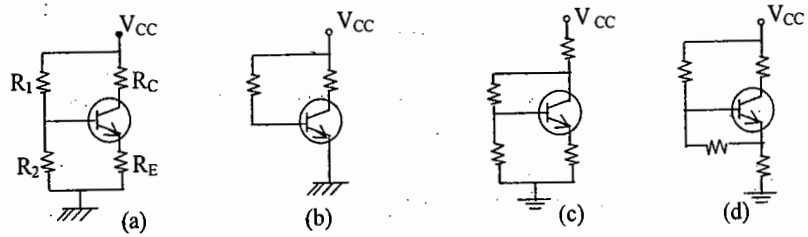


9. For good stabilized biasing of the transistor of the CE amplifier shown below, the condition is

a) $\frac{R_E}{R_B} << 1$ b) $\frac{R_E}{R_B} >> 1$
c) $\frac{R_B}{R_E} << h_{FE}$ c) $\frac{R_B}{R_E} >> h_{FE}$




10. Of the four biasing circuits shown in figure for a BJT, indicate the one which can have maximum bias stability.



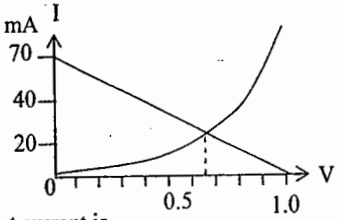

11. The quiescent collector current $I_C$ of a transistor is increased by changing the biasing resistances. As a result $g_m$ will
a) not be affected b) decrease c) increase
d) increase or decrease depending on bias stability.

12. Pick out the correct statements
a) DC load line is same as AC load line b) DC load line is steeper than AC load line
c) AC load line is steeper than DC load line
d) AC signal swing is restricted in an AC load line

13. The parameters that can be determined from a load line are
a) quiescent point only
b) quiescent point, Thevenin voltage, Norton current
c) quiescent point, no load voltage, short circuit current, voltage drop across load
d) in addition to parameters in (c) above, voltage drop across device

For Questions 14 to 17, the figure shows V – I characteristic and load line of a nonlinear device in series with a load resistor

14. With reference to the figure the cut in voltage of the device is
a) 0.65
b) 0.1
c) 0.5
d) 0



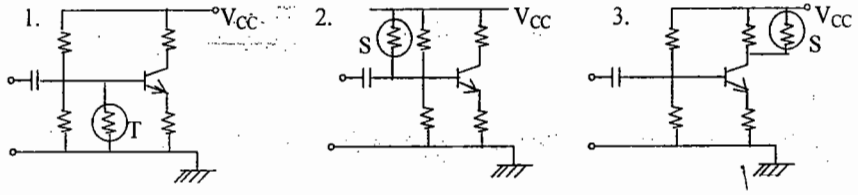

15. With reference to the above figure the quiescent current is
a) 70mA, b) 0 c) 20 mA d) 23mA

16. With reference to the above figure, the voltage across the non-linear device is
a) 1V b) 0.65V c) 0.35V d) 0.5 V

17. With reference to the above figure, the drop across the load resistor is

a) 0.35 V b) 0.65V c) 1V d) 0V

18. Which of the following circuits realize self bias with compensation?

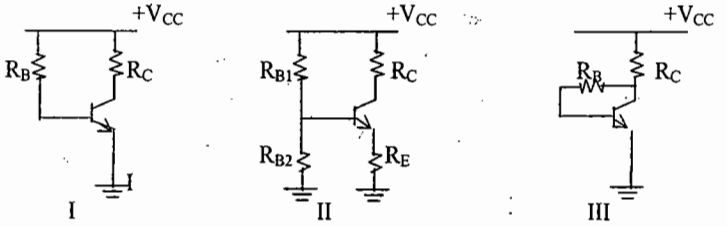



T = Thermistor, S = Sensistor

Select the correct answer using the codes given below:

a) 2 and 3 b) 1 and2 c) 1 and 3 d) 1,2 and 3

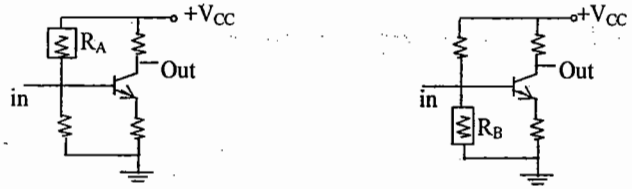
19. Three different circuits for biasing junction transistor amplifiers are given below




The correct decreasing order of preference of these circuits from the point of view of bias stabilisation is

a) I, II, III b) III, II, I c) II, III, I d) I, III, II

20. In the following two non-linear transistor biasing circuits, the resistors,




a) $R_A$ and $R_B$, both have negative temperature coefficients
b) $R_A$ and $R_B$, both have positive temperature coefficients
c) $R_A$ has negative temperature coefficient and $R_B$ has Positive temperature coefficient
d) $R_A$ has positive temperature coefficient and $R_B$ has Negative temperature coefficient.

**KEY:**

**1. d 2.c 3.c 4.a 5.c 6.d 7.b 8.c 9.b 10.a 11.c 12.c**

**13.d 14.c 15.d 16.b 17.a 18.b 19.c 20.d**

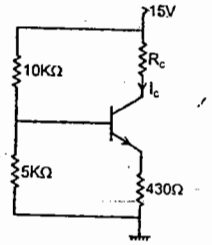


## SET - B

01. In the circuit of the figure, assume that the transistor is in the active region. It has a large β and its base – emitter voltage is 0.7 V. The value of $I_C$ is

(A) indeterminate since $R_C$ is not given

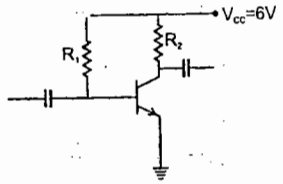
(B) 1 mA (C) 5 mA (D) 10 mA




02. In the amplifier circuit shown in the figure, the values of $R_1$ and $R_2$ are such that the transistor is operating at $V_{CE}$ = 3 V and $I_C$ = 1.5 mA when its β is 150. For a transistor with β of 200, the operating point ($V_{CE}$, $I_C$) is

(A) (2V, 2mA) (B) (3V, 2mA)

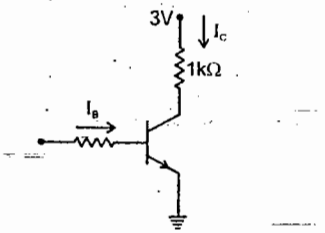
(C) (4V, 2mA) (D) (4V, 1mA)




03. Assuming $V_{CEsat}$ = 0.2 V and β = 50, the minimum base current ($I_B$) required to drive the transistor in the figure to saturation is

(A) 56 μA (B) 140 μA

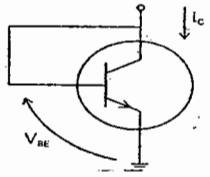
(C) 60 μA (D) 3 mA



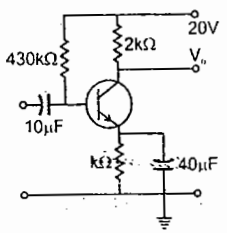

04. For an npn transistor connected as shown in the figure, VBE = 0.7 volts. Given that reverse saturation current of the junction at room temperature 3000 K is 10-13 A, the emitter current

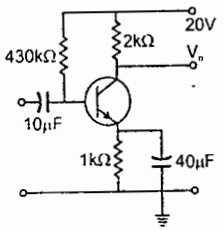
(A)30mA (B)39mA

(C) 49mA (D)20 mA



05. The circuit using a HJT with β - 50 and $V_{BE}$ = 0.7 V is shown in the figure. The base current $I_B$ and collector voltage $V_C$ are respectively




(A) 43 μA and 11.4 Volts

(B) 40 μA and 16 volts

(C) 45 μA and 11 Volts

(D) 50 μA and 10 Volts

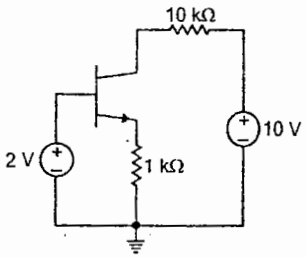
06. For the BJT circuit shown, assume that the β of the transistor is very large and $V_{BE}$ = 0.7 V. The mode of operation of the BJT

(A) cut – off

(B) saturation

(C) normal active

(D) reverse active




07. Introducing a resistor in the emitter of a common amplifier stabilizes the dc operating point against variations in

(A) only the temperature

(B) only the β of the transistor

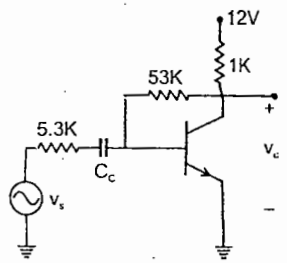
(C) both temperature and β

(D) none of the above



**Common data for Questions 08, 09 and 10.**

In the transistor amplifier circuit shown in the figure below, the transistor has the following parameters: $\beta_{DC}$ = 60, $V_{BE}$ = 0.7 V, $h_{ie} \to \infty$, $h_{fe} \to \infty$ The capacitance $C_C$ can be assumed to be infinite. In the figure above, the ground has been shown . By the symbol ∇




08. Under the DC conditions, the collector – to – emitter voltage drop is

(A) 4.8 Volts (B) 5.3 Volts (C) 6.0 Volts (D) 6.6 Volts

09. If $\beta_C$ is increased by 10%, the collector – to – emitter voltage drop

(A) increases by less than or equal to 10%

(B) decreases by less than or equal to 10%

(C) increases by more than 10%

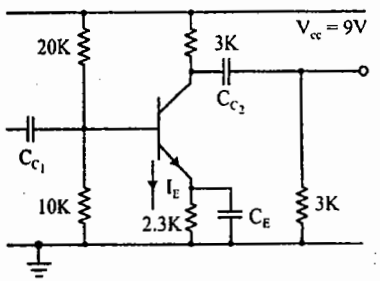
(D) decreases by more than 10%

10. The small – signal gain of the amplifier $V_C/V_S$ is

(A) – 10 (B) – 5.3 (C) 5.3 (D) 10

**Statement for linked answer Questions 11 & 12.**

In the following transistor circuit, $V_{BE} = 0.7$ V, $r_e = 25\ mV/I_E$, and $\beta$ and all the capacitances are very large




11. The value of DC current $I_E$ is

(A) 1 mA (B) 2 mA

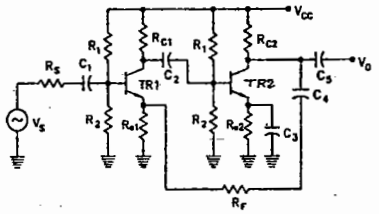
(C) 5 mA (D) 10 mA

12. The mid – band voltage gain of the amplifier is approximately

(A) – 180 (B) – 120

(C) – 90 (D) – 60

13. Given figure shows a two – state small signal transistor feedback amplifier. Match the defective component in list – I with its probable effect on the circuit in list - II




List – I

(A) Capacitor $C_1$ is open

(B) Capacitor $C_3$ is open

(C) Capacitor $C_4$ is open

(D) $Rc_2$ is shorted

List – II

P. all dc voltages normal normal, $v_0$ increases marginally

Q. collector of TRZ is at $V_{CC}$, $v_0 = 0$

R. all dc voltages normal, gain of 2nd stage increase $v_0$ decrease

S. all dc voltages normal, $v_0 = 0$

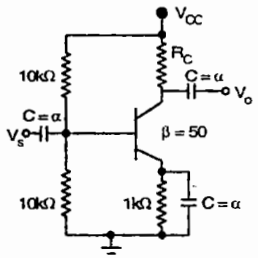
T. all dc voltages normal, overall gain of the amplifier increases, $v_0$ increases

U. No change

14. The transconductance $g_m$ of the transistor shown in figure is 10 mS. The value of the input resistance $R_{IN}$ is

(A) 10.0 kΩ (B) 8.3 k Ω

(C) 5.0 k Ω (D) 2.5 kΩ




**KEY: SET - B**

| | | | | | |
|---|---|---|---|---|---|
| (1) D | (2) A | (3) A | (4) C | (5) B | (6) B |
| (7) C | (8) C | (9) B | (10) A | (11) A | (12) D |
| (13) a – S, b – R, c – T, D – Q | | | (14) D | | |



## FET BIASING

For the field-effect transistor the relationship between input and output quantities is non-linear due to the squared term in Schockley's equation. This non-linear relationship between $I_D$ and $V_{GS}$ can complicate the mathematical approach to the dc analysis of FET configuration. A graphical approach may limit solutions to tenths place accuracy but it is a quicker method for most FET amplifiers.

Another distinct difference between the analysis of BJT and FET transistors is that the input controlling variable for a BJT transistor is a current level, while for the FET a voltage is the controlling variable. In both cases, however, the controlled variable on the output side is a current level that also defines the important voltage levels of the output circuit. The general relationships that can be applied to the dc analysis of all FET amplifiers are

$$I_G \cong 0A$$

and $I_D = I_S$

For JFETs and depletion-type MOSFETs shockley's equation is applied to relate the input and output quantities:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

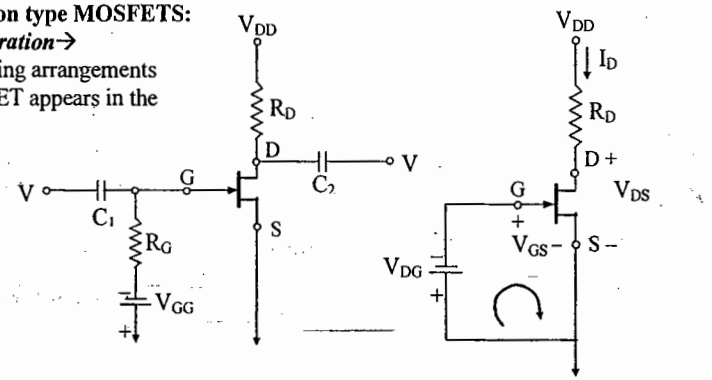
For enhancement-type MOSFETs the following equation is applicable:

$$I_D = K(V_{GS} - V_T)^2$$

**JFETs and Depletion type MOSFETS:**

***Fixed Bias Configuration→***

The simplest of biasing arrangements for the n-channel JFET appears in the following figures




The configuration includes the ac levels $V_i$ and $V_0$ and the coupling capacitors ( $C_1$ and $C_2$). The coupling capacitors are "open circuits" for the dc analysis and low impedances for the ac analysis. The resistor $R_G$ is present to ensure that $V_i$ appears at the input to the- JFET amplifier for the ac analysis.

For the dc analysis

$$I_G \cong 0A$$

and $V_{RG} = I_G R_G = (0A) R_G = 0V$

Applying KVL in the clockwise direction of the indicated loop will result in

$$-V_{GG} - V_{GS} = 0$$

and $V_{GS} = -V_{GG}$

Since $V_{GG}$ is a fixed dc supply the voltage $V_{GS}$ is fixed in magnitude, resulting in the notation " fixed-bias configuration".

The resulting level of drain current $I_D$ is now controlled by shockley's equation:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

The drain-to-source voltage of the output section can be determined by applying kirchoff's voltage low as follow:

$$+V_{DS} + I_D R_D - V_{DD} = 0$$

and $$\boxed{V_{DS} = V_{DD} - I_D R_D}$$

For the configuration of the given figure, $\boxed{V_S = 0V}$

Using double-subscript notation:

$$V_{DS} = V_D - V_S$$
$$V_D = V_{DS} + V_S = V_{DS} + 0V$$

and $$\boxed{V_D = V_{DS}}$$

In addition, $V_{GS} = V_G - V_S$

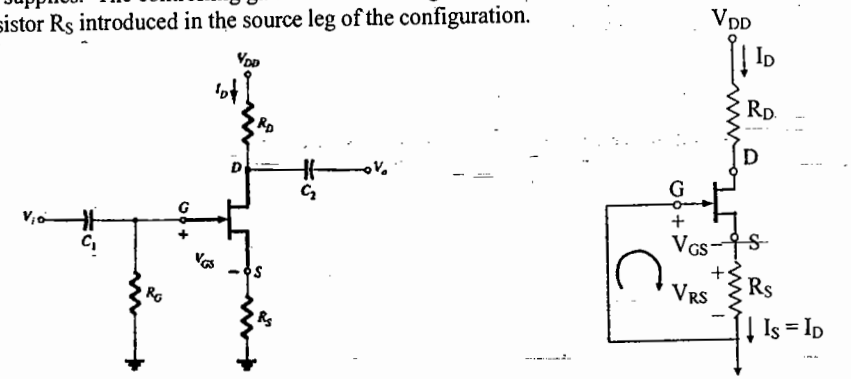
$$V_G = V_{GS} + V_S = V_{GS} + 0V$$

and $\boxed{V_G = V_{GS}}$

Since the configuration requires two dc supplies, its use is limited.

***SELF BIAS CONFIGURATION→***

The self-bias configuration eliminates the need for two dc supplies. The controlling gate-to-source voltage is now determined by the voltage across a resistor $R_S$ introduced in the source leg of the configuration.




For the dc analysis the capacitors can again be replaced by "open circuits" and the resistor $R_G$ replaced by a short circuit equivalent since $I_G = 0A$.

The current through $R_S$ is the source $I_S$, but $I_S = I_D$ and $V_{RS} = I_D R_S$

For the indicated closed loop,

$$-V_{GS} - V_{RS} = 0$$

and $$V_{GS} = -V_{RS}$$

or $$\boxed{V_{GS} = -I_D R_S}$$



Note in this case that $V_{GS}$ is a function of the output current $I_D$ and not fixed in magnitude as occurred for the fixed-bias configuration.

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$
$$= I_{DSS}\left(1 + \frac{I_D R_S}{V_P}\right)^2$$

The quadratic equation can be solved for the appropriate solution for $I_D$

Applying Kirchoff's voltage law to the output circuit,

$$V_{RS} + V_{DS} + V_{RD} - V_{DD} = 0$$

and $$V_{DS} = V_{DD} - V_{RS} - V_{RD}$$
$$= V_{DD} - I_S R_S - I_D R_D$$

but $I_D = I_S$

and $V_{DS} = V_{DD} - I_D (R_S + R_D)$

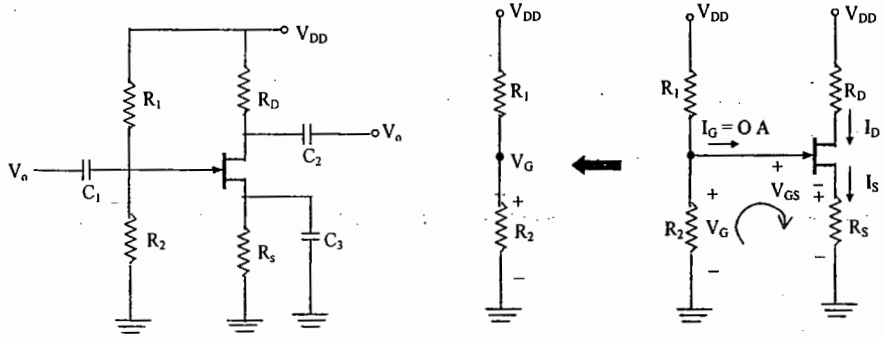
In addition: $V_S = I_D R_S$

$V_G = 0V$

and $V_D = V_{DS} + V_S = V_{DD} - V_{RD}$

***VOLTAGE – DIVIDER BIASING→***

The voltage divider bias arrangement applied to BJT transistor amplifiers is also applied to FET amplifiers. The base construction is exactly the same, but the dc analysis of each is quite different. $I_G = 0A$ for FET amplifier, but the magnitude of $I_B$ for common-emitter amplifiers can affect the dc levels of current and voltage in both the input and output circuits. $I_B$ provided the link between input and output circuits for the BJT voltage-divider configuration while $V_{GS}$ will do the same for the FET configuration




All the capacitors, including the by pass capacitor $C_S$, have been replaced by an "open circuit" equivalent. In addition, the source $V_{DD}$ was separated into two equivalent sources to permit a further separation of the input and output regions of the network.

Since $I_G = 0A$, Kirchoff's current law requires that $I_{R1} = I_{R2}$ using voltage divider rule:

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$$

Applying KVL in the clockwise direction to the indicated loop

$$V_G - V_{GS} - V_{RS} = 0$$

$$V_{GS} = V_G - V_{RS}$$

or $$\boxed{V_{GS} = V_G - I_D R_S}$$

Applying graphical analysis, $V_{GS} = V_G \big|_{I_D = 0mA}$

$$I_D = \frac{V_G}{R_S}\Big|_{V_{GS} = 0V}$$

The two points defined above permit the drawing of a straight line to represent the equation. The intersection of the straight line with the transfer curve in the region to the left of the vertical axis will define the operating point and the corresponding levels of $I_D$ and $V_{GS}$.

Once the quiescent values of $I_{DQ}$ and $V_{GSQ}$ are determined, the remaining network analysis can be performed in the usual manner. That is,

$$V_{DS} = V_{DD} - I_D (R_D + R_S)$$
$$V_D = V_{DD} - I_D R_D$$
$$V_S = I_D R_S$$

$$I_{R1} = I_{R2} = \frac{V_{DD}}{R_1 + R_2}$$

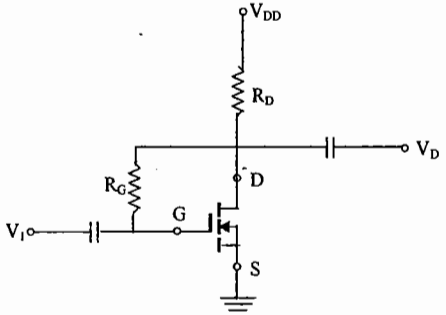
The similarities in appearance between the transfer curves of JFETs the depletion type MOSFETs permit a similar analysis of each in the dc domain. The primary difference between the two in the fact that depletion type MOSFETs permit operating points with positive values of $V_{GS}$ and levels of $I_D$ that exceed $I_{DSS}$. In fact, for all the configurations discussed thus for, the analysis is the same if the JFET is replaced by a depletion-type MOSFET.

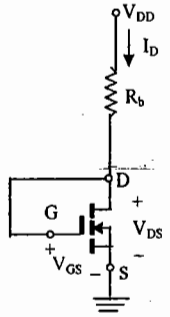
*ENHANCEMENT TYPE MOSFETS*

The transfer characteristics of the enhancement type MOSFET are quite different from those encountered for the JFET and depletion type MOSFETs resulting in a graphical solution quite different from the preceding sections. For the n-channel enhancement-type MOSFET, the drain current is zero for levels of gate-to-source voltage less than the threshold level $V_{GS(Th)}$. For levels of $V_{GS}$ greater than $V_{GS(Th)}$, the drain current is defined by $I_D = K(V_{GS} - V_{GS(Th)})^2$ where

$$K = \frac{I_{D(on)}}{(V_{GS(on)} - V_{GS(Th)})^2}$$

*FEED BACK BIASING ARRANGEMENT→*






The resistor $R_G$ brings a suitably large voltage to the gate to drive the MOSFET "on".

$I_G = 0mA$ and $V_{RG} = 0V$ for the dc equivalent network.

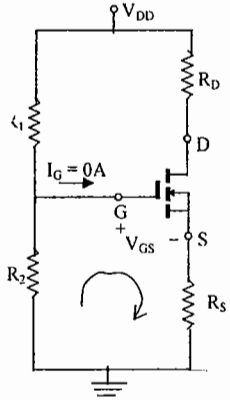
A direct connection now exists between drain and gate, resulting in $V_D = V_G$ and $\boxed{V_{DS} = V_{GS}}$

For the output circuit, $\boxed{V_{GS} = V_{DD} - I_D R_D}$

Since the above equation is that of a straight line, the points $V_{GS} = V_{DD}\big|_{I_D = 0mA}$ and $I_D = \frac{V_{DD}}{R_D}\Big|_{V_{GS} = 0V}$

determine the two points that will define the plot on the graph.

*VOLTAGE – DIVIDER BIASING ARRANGEMENT→*




The fact that $I_G = 0mA$ results in the following equation for $V_{GG}$ as derived from an application of the voltage-divider rule

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$$

Applying KVL around the indicated loop

$$+V_G - V_{GS} - V_{RS} = 0$$

and $V_{GS} = V_G - V_{RS}$

or $\boxed{V_{GS} = V_G - I_D R_S}$

For the output section:

$$V_{RS} + V_{DS} + V_{RD} - V_{DD} = 0$$

and $V_{DS} = V_{DD} - V_{RS} - V_{RD}$

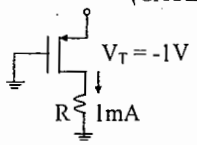
or $V_{DS} = V_{DD} - I_D (R_S + R_D)$

since the characteristics are a plot of $I_D$ versus $V_{GS}$ and the above equation relates the same two variables, the two curves can be plotted on the same graph and a solution determined at their intersection. Once $I_{DQ}$ and $V_{GSQ}$ are known, all the remaining quantities of the network such as $V_{DS}$, $V_D$ and $V_S$ can be determined.

## OBJECTIVES QUESTIONS - FET BIASING

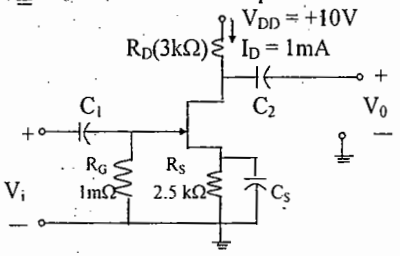
1. An n-channel JFET, having a pinch off voltage ($V_P$) of -5V shows a transconductance (gm) of 1mA/V when the applied gate-to-source voltage ($V_{GS}$) is –3V. Its maximum transconductance (in mA/V) is *(GATE 2001, EEE)*
a) 1.5 b) 2.0 c) 2.5 d) 3.0

2. The value of R for which the PMOS transistor in figure will be biased in linear region is *(GATE 2004, EEE)*
+4V
a) 220Ω
b) 470Ω
c) 680Ω
d) 1200Ω




3. The action of a JFET in its equivalent circuit can best be represented as a *(GATE 2003, ECE)*
a) current controlled current source b) current controlled voltage source
c) voltage controlled voltage source d) voltage controlled current source

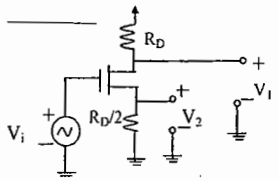
4. The voltage gain $A_V \triangleq V_0 / V_i$ of the JFET amplifier *(GATE 02, ECE)*
a) +18
b) –18
c) +6
d) –6



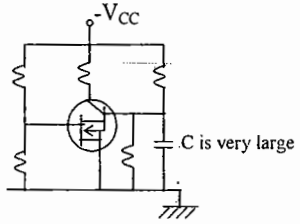

$I_{SS}$ = 10 mA
$V_P$ = - 5V
(Assume $C_1$, $C_2$, $C_S$ to be very large)

5. Two identical FETs each characterized by the parameter gm and rd are connected in parallel.The composite FET is then characterized by the parameter. *(GATE 98, ECE)*
a) $g_m/2$ and $2r_d$ b) $g_m/2$ and $r_{d/2}$ c) $2g_m$ and $r_{d/2}$ d) $2g_m$ and $2r_d$

06. In the MOSFET amplifier, the signal outputs $V_1$ and $V_2$ obey the relationship *(GATE 98, ECE)*
a) $V_1 = V_2 / 2$
b) $V_1 = -V_2 /2$
c) $V_1 = 2V_2$
d) $V_1 = -2V_2$




7 The given figure shows a composite transistor continuity of a MOSFET and a bipolar transistor in cascade. The MOSFET has a transconductance gm of 2mA/V and the bipolar transistor has β ($\Delta h_{fe}$) of 99. The overall transconductance of the composite transistor is *(IES 99, ECE)*
a) 198 mA/V
b) 19.8 mA/V
c) 1.98 A/V
d) 1.98 mA/V






8. For an n-channel JFET, having drain-source voltage constant if the gate-source Voltage is increased (more negative) pinch-off would occur for
a) High values of drain current b) Saturation values of drain current
c) Zero drain current d) Gate current equal to drain current

9. In modern MOSFETs, the material used for the gate is
a) High quality silicon b) High purity silica
c) Heavily doped polycrystalline silicon d) Epitaxial grown silicon

10. The pinch-off voltage of a JFET is 5.0 volts. Its "cut-off" voltage is
a) $(5.0)^{1/2}$ b) 2.5V c) 5.0V d) $(5.0)^{3/2}$

11. The transconductance $g_m$ of a FET in the saturation region equals:
a) $\frac{-2I_{DSS}}{V_P}\left(1-\frac{V_{GS}}{V_P}\right)$ b) $\frac{-2I_{DSS}}{V_P}\left(1-\frac{V_{GS}}{V_P}\right)^2$
c) $2I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)^{1/2}$ d) $\frac{1}{V_P(I_{DSS}-I_{DS})^{1/2}}$

12. Consider the following statements:
Threshold voltage of a MOSFET can be lowered by
1) Using a thinner gate oxide 2) Reducing the substrate connection
3) Increasing the substrate connection
Of these statements:
a) 3 alone is correct b)1 and 2 are correct
c) 1 and 3 are correct d) 2 alone is correct

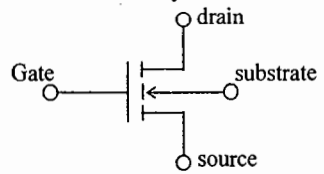
13.Consider the following devices:
1. BJT in CB mode 2.BJT in CE mode 3.JFET 4.MOSFET
The correct sequence of the devices in increasing order of their input impedances is:
a) 1,2,3,4 b) 2,1,3,4 c) 2,1,4,3 d) 1,3,2,4

14. Match the items given in List- I(structures/characteristics) with List- II(Reasons) in respect of JFET and Select the correct answer using the codes given below the lists:

| List-I | List-II |
|---|---|
| A. N-channel JFET is better than P-channel JFET | 1. Reverse bias increases the channel |
| B. Channel is wedge shaped | 2. High electric field near the drain and directed towards source |
| C. Channel is not completely closed at pinch-off | 3. Low leakage current at the gate terminal |
| D. Input impedance is high | 4. Better frequency performance |

Code:
a) A-4, B-1,C- 2, D - 3 b) A-4, B-2, C -1,D-3
c) A-3,B-1,C -2 ,D- 4 d) A-3, B-2,C- 1,D- 4

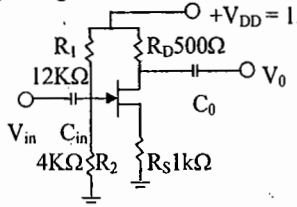
15. The below Fig. Shows the circuit symbol of




a) FET b) PMOS FET c) MOS FET d) NMOS FET

16. The output current versus input voltage transfer characteristic of an n-channel JFET is Such that there is
a) Zero current flow at zero input voltage bias
b) Current flow only when a positive input threshold voltage is crossed
c) Current flow only when a negative input cut-off voltage bias is crossed
d) No cut-off input voltage

17. A JFET circuit using voltage-divider bias is shown in fig.The gate voltage is




a) 3.55V b) 3.65V c) 3.75V d) 3.85V

18. A JFET has a potential divider bias arrangement, if the resistor between the gate and power supply terminal is removed. The JFET will
a) continue to work as an amplifier
b) have a forward bias gate w.r.t. source
c) not work as an amplifier but will work as switch
d) immediately burn out

19. An n-channel JFET has $I_{DS}$ whose value is
a) maximum for $V_{GS}$=0, and minimum for $V_{GS}$= negative and large
b) minimum for $V_{GS}$=0, and maximum for $V_{GS}$= negative and large
c) maximum for $V_{GS}$=0, and minimum for $V_{GS}$= positive and large
d) minimum for $V_{GS}$=0, and maximum for $V_{GS}$= positive and large

**KEY:** **1. c 2.d 3.d 4.d 5.c 6.a 7.d 8. c 9. c**
**10. c 11. a 12. c 13. a 14. a 15. d 16. c 17. c 18. a**
**19. a**



One of our first concerns in the sinusoidal ac analysis of transistor networks is the magnitude of the input signal. It will determine whether small signal or large signal techniques should be applied. There is no set dividing line between the two, but the application, and the magnitude of the variables of interest relative to the scales of the device characteristics, will usually make it quite clear which method is appropriate.

There are two models commonly used in the small-signal ac analysis of transistor networks. The $r_e$ model and the hybrid equivalent model.

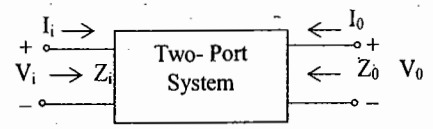
It is indeed fortunate that transistor small signal amplifiers can be considered linear for most applications, permitting the use of the superposition theorem to isolate the dc analysis from the ac analysis.

**BJT TRANSISTOR MODELING→**

A model is the combination of circuit elements, properly chosen, that best approximates the actual behavior of a semi conductor device under specific operating conditions. Once the ac equivalent circuit has been determined the graphic symbol of the device can be replaced in the schematic by this circuit and the basic methods of ac circuit analysis (mesh analysis, nodal analysis, and Thevenin's theorem) can be applied to determine the response of the circuit. The $r_e$ model equivalent circuit is derived directly from the operating conditions of the transistor while the hybrid equivalent circuit suffers from being limited to a particular set of operating conditions if it is to be considered accurate. In turn, however, the $r_e$ model fails to account for the output impedance level of the device and the feedback effect from output to input.

The ac equivalent of a network is obtained by setting all dc sources to zero and replacing them by a short circuit equivalent

***THE IMPORTANT PARAMETERS***: $Z_i$ , $Z_0$, $A_V$, $A_i$




Input impedance, $Z_i$ →

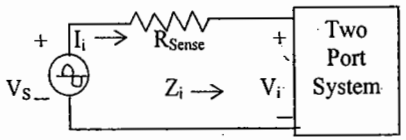
For the input side, the input impedance $Z_i$ is defined by Ohm's law as the following:

$$Z_i = \frac{V_i}{I_i}$$

For small-signal analysis, once the input impedance has been determined the same numerical value can be used for changing levels of applied signals. The input impedance of a BJT transistor amplifier is purely resistive in nature, and depending on the manner, in which the transistor is employed, can vary from a few ohms to megaohms.

The input impedance is then determined in the following manner:

$$I_i = \frac{V_S - V_i}{R_{Sense}} \qquad Z_i = \frac{V_i}{I_i}$$

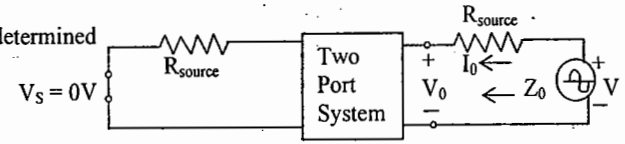



The level of the input impedance can have a significant impact on the level of signal that reaches the system.

**Output Impedance, $Z_0$ →**

The output impedance is determined at the output terminals looking back into the system with the applied signal set to zero.

The output impedance is determined by $I_0 = \frac{V - V_0}{R_{Sense}}$ and $Z_0 = V_0 / I_0$



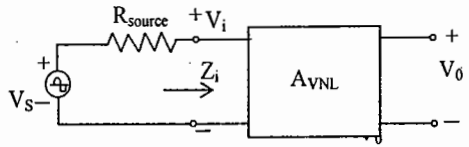

The output impedance of a BJT amplifier is resistive in nature and depending on the configuration and the placement of the resistive elements, $Z_0$, can vary from a few ohms to a level that can exceed 2MΩ.

An ohmmeter cannot be used to measure the small signal ac input and output impedance since the ohmmeter operates in the dc mode.

**Voltage Gain, $A_V$ →**

One of the most important characteristics of an amplifier is the small signal ac voltage gain as determined by $A_V = V_0 / V_i$

The no load voltage gain, $A_{VNL} = \left.\frac{V_0}{V_i}\right|_{R_L = \infty\Omega}$




For transistor amplifiers, the no load voltage gain is greater than the loaded voltage gain For the system having a source resistance $R_s$.

$$A_{VS} = \frac{V_0}{V_S} = \frac{Z_i}{Z_i + R_S} A_{VNL}$$

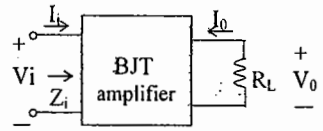
Depending on the configuration, the magnitude of the voltage gain for a loaded single-stage transistor amplifier typically ranges from just less than 1 to a few hundred. A multi Stage system, however, can have a voltage gain in the thousands.



**Current Gain, $A_i$ →** $A_i = \frac{I_0}{I_i}$

For BJT amplifiers, the current gain typically ranges from a level just less than 1 to a level that may exceed 100.

For the loaded situation $I_i = \frac{V_i}{Z_i}$ and $I_0 = \frac{-V_0}{R_L}$




$$A_i = \frac{I_0}{I_i} = -\frac{V_0 / R_L}{V_i / Z_i} = -\frac{V_0}{V_i}\frac{Z_i}{R_L}$$

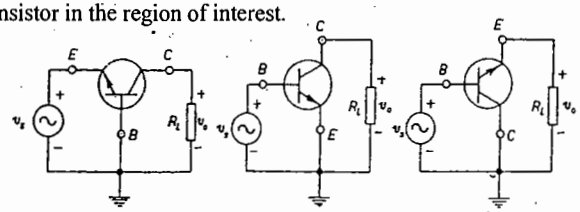
$$A_i = -A_v Z_i / R_L$$

**Phase Relationship →**

The phase relationship between input and output sinusoidal signals is important for a variety of practical reasons. Fortunately, however; for the typical transistor amplifier at frequencies that permit ignoring the effects of the reactive elements, the input and output signals are either 180° out of phase or in phase.

**THE $r_e$ TRANSISTOR MODEL →**

The $r_e$ model employs a diode and controlled current source to duplicate the behaviour of a transistor in the region of interest.




**Common Base Configuration:**

One junction of an operating transistor is forward biased while the other is reverse biased. The forward biased junction will behave much like a diode. For the base to emitter junction of the transistor the diode equivalence between the same two terminals seems to be quite appropriate. For the output side, $I_c \cong I_e$ ( as derived from $I_c = \alpha I_e$) for the range of values of $V_{CE}$. The current source establishes the fact that $I_C = \alpha I_e$ with the controlling current $I_e$ appearing in the input side of the equivalent circuit. We have therefore established an equivalence at the input and output terminals with the current- controlled source, providing a link between the two.

The ac resistance of the diode, $r_e = \frac{26mV}{I_E}$

Due to the isolation that exists between input and output circuits it should be fairly obvious that the input impedance $Z_i = r_e$

CB configuration: Typical values of $Z_i$ range from a few ohms to a maximum of about 50Ω.
The output impedance $\boxed{Z_0 \cong \infty\,\Omega}$

In actuality for the CB configuration, typical values of $Z_0$ are in the mega ohm range.
In general, for the common base configuration the input impedance is relatively small and the output impedance quite high.

Voltage gain. $A_v = \frac{V_0}{V_i} = \frac{-(I_0 R_L)}{(I_e r_e)} = \frac{-(-I_C)R_L}{(I_e r_e)} = \frac{\alpha I_e R_L}{I_e r_e}$

$$\boxed{A_v = \frac{\alpha R_L}{r_e} \cong \frac{R_L}{r_e}}$$

Current gain,

$$A_i = \frac{I_0}{I_i} = \frac{-I_C}{I_e} = \frac{-\alpha I_e}{I_e}$$

$V_0$ and $V_i$ are in phase for CB configuration

$\boxed{A_i = -\alpha \cong -1}$ CB

***Common Emitter Configuration:***

The controlled – current source is still connected between the collector and base terminals and the diode between the base and emitter terminals. In this configuration, the base current is the input current, while the output current is still $I_c$.

$I_c = \beta I_b$

The current through the diode $I_e = I_c + I_b = \beta I_b + I_b$

$I_e = (\beta+1) I_b$

However, since the ac beta is typically much greater than 1,

$I_e \cong \beta I_b$

Input impedance, $Z_i = \frac{V_i}{I_i} = \frac{-V_{be}}{I_b} \simeq \frac{\beta I_b r_e}{I_b}$

$\boxed{Z_i \cong \beta r_e}$

In other words, a resistive element in the emitter leg is reflected into the input circuit by a multiplying factor β.

Output impedance, $\boxed{Z_0 = r_0}$. If the contribution due to $r_0$ is ignored the output impedance is defined by $Z_0 = \infty\,\Omega$.

Voltage gain, $A_v = \frac{V_0}{V_i}$

$\boxed{= -R_L / r_e}$,

$r_0 = \infty\Omega$



The resulting minus sign for the voltage gain reveals that the output and input voltages are 180° out of phase.

Current gain, $A_i = \frac{I_0}{I_i} = \frac{I_c}{I_b} = \frac{\beta I_b}{I_b}$

and $\boxed{A_i = \beta}$,

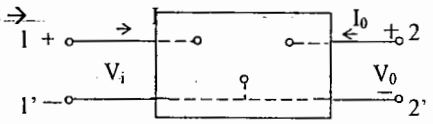
$r_0 = \infty\Omega$

**Common collector configuration:** For the common collector configuration, the model defined for the common – emitter configuration is normally applied.

**THE HYBRID EQUIVALENT MODEL →**

$V_i = h_{11} I_i + h_{12} V_0$

$I_0 = h_{21} I_i + h_{22} V_0$




The parameter relating the four variables are called h – parameters from the word "hybrid". The term hybrid was chosen because the mixture of variables (V and I) in each equation results in a "hybrid" set of units of measurements for the h – parameters.

$$h_{11} = \left.\frac{V_i}{I_i}\right|_{V_0 = 0} \text{ ohms}$$

The ratio indicates that the parameter $h_{11}$ is an impedance parameter with the units of ohms. Since it is the ratio of the input voltage to the input current with the output terminals shorted, it is called the short circuit input impedance parameter.

$$h_{12} = \left.\frac{V_i}{V_0}\right|_{I_i = 0} \text{ unit-less.}$$

The parameter $h_{12}$, therefore, is the ratio of the input voltage to the output voltage with the input current equal to zero.It has no units since it is a ratio of voltage levels and is called the open – circuit reverse transfer voltage ratio parameter.

$$h_{21} = \left.\frac{I_0}{I_i}\right|_{V_0 = 0} \text{ unit-less}$$

The parameter $h_{21}$ is the ratio of the output current to the input current with the output terminals shorted. This parameter has no units since it is the ratio of current levels. It is formally called the short – circuit forward transfer current ratio parameter.

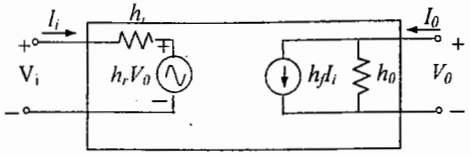
$$h_{22} = \left.\frac{I_0}{V_0}\right|_{I_i = 0} \text{ Siemens}$$

Since it is the ratio of the output current to the output voltage, it is the output conductance parameter and is measured in Siemens(S). It is called the open circuit output admittance parameter.

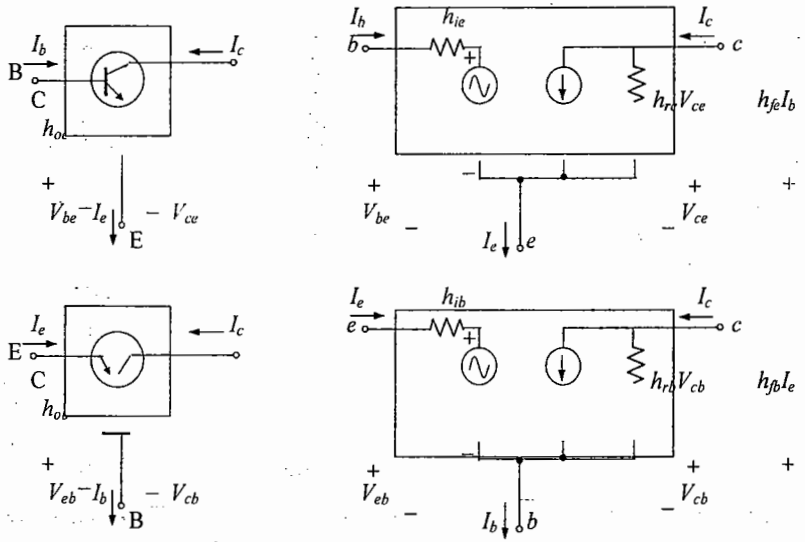
Apply Kirchoff's voltage law "in reverse" to find the input circuit. Since the parameter $h_{11}$ has the unit ohm, it is represented by a resistor. The quantity $h_{12}$ is dimensionless and therefore simply appears as a multiplying factor of the "feed back" term in the input circuit.

Apply Kirchoff's current law "in reverse' to obtain the output circuit. Since $h_{22}$ has the units of admittance, which for the transistor model is conductance, it is represented by the resistor symbol. Whose value is equal to $h_0$.

$h_{11}$ = input resistance → $h_i$
$h_{12}$ = reverse transfer voltage ratio → $h_r$
$h_{21}$ = forward transfer current ratio → $h_f$
$h_{22}$ = output conductance → $h_0$




The above circuit is applicable to any linear three terminal electronic device or system with no internal independent sources. For the transistor, therefore, even though it has three basic configurations, they are all three – terminal configurations, so that the resulting equivalent circuit will have the same format. The h parameter, however, will change with each configuration.



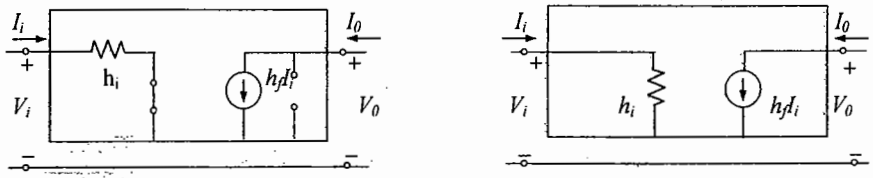

For the CE configuration, $I_i = I_b$, $I_0 = I_c$ and through an application of Kirchoff's current law, $I_e = I_b + I_c$. The input voltage is now $V_{be}$ with the output voltage $Vc_e$.

For the CB configuration, $I_i = I_e$, $I_0 = I_e$ with $V_{eb} = V_i$ and $Vc_b = V_0$. The above networks are applicable for pnp as well npn transistors.

For the CE and CB configurations the magnitude of $h_r$ and $h_0$ is often such that the results obtained for the important parameter such as $Z_i$, $Z_0$, $A_v$ and $A_i$ are only slightly affected if they ($h_r$ and $h_0$) are not included in the model.

Since $h_r$ is normally a relatively small quantity, its removal is approximated by $h_r \cong 0$ and $h_r V_0 = 0$, resulting in a short circuit equivalent for the feed back element. The resistance determined by $1/h_0$ is often large enough to be ignored in comparison to a parallel load permitting its replacement by an open – circuit equivalent for the CE and CB models.






Also note the relationship between the hybrid and $r_e$ – models.

$h_{ie} = \beta r_e$
and $h_{fc} = \beta_{ac}$
$h_{ib} = r_e$

and $h_{fb} = -\alpha \cong -1$. The minus sign accounts for the fact that the current source of the standard hybrid model is putting down rather than in the actual direction in the $r_e$ model.

The hybrid parameter $h_{fe}$ ($\beta_{ac}$) is the least sensitive of the hybrid parameters to a change in collector circuit. Assuming, therefore that $h_{fe} = \beta$ is a constant for the range of interest is a fairly good approximation. It is $h_{ie} = \beta r_e$ that will vary significantly with $I_C$ and should be determined at operating levels, since it can have a real impact on the gain levels of a transistor amplifier.

**The approximate relations between the parameters are given below:**
**Common – Emitter Configuration**

$$h_{ie} \cong \frac{h_{ib}}{1 + h_{fb}} \cong \beta r_e$$

$$h_{re} \cong \frac{h_{ib} h_{ob}}{1 + h_{fb}} - h_{rb}$$

$$h_{fe} \cong \frac{-h_{fb}}{1 + h_{fb}} \cong \beta$$

$$h_{oe} \cong \frac{h_{ob}}{1 + h_{fb}}$$

**Common-Base Configuration**

$$h_{ib} \cong \frac{h_{ie}}{1 + h_{fe}} \cong \frac{-h_{ic}}{h_{fc}} \cong r_e$$

$$h_{rb} \cong \frac{h_{ie} h_{oe}}{1 + h_{fe}} - h_{re} \cong h_{rc} - 1 - \frac{h_{ic} h_{oc}}{h_{fc}}$$

$$h_{fb} \cong \frac{-h_{fe}}{1 + h_{fc}} \cong \frac{-(1+h_{fc})}{h_{fc}} \cong -\alpha$$

$$h_{ob} \cong \frac{h_{oe}}{1 + h_{fe}} \cong \frac{-h_{oc}}{h_{fc}}$$

**Common-Collector Configuration**

$$h_{ic} \cong \frac{h_{ib}}{1 + h_{fb}} \cong \beta r_e$$

$$h_{rc} \cong 1$$

$$h_{fc} \cong \frac{-1}{1 + h_{fb}} \cong -\beta$$

$$h_{oc} \cong \frac{h_{ob}}{1 + h_{fb}}$$

**Characteristics of Common Base Amplifier**

- Current gain is less than unity and its magnitude decreases with the increase of load resistance $R_L$
- Voltage gain $Av$ is high for normal values of $R_L$
- The input resistance $R_i$ is the lowest of all the three configurations, and
- The output resistance $Ro$ is the highest of all the three configurations. ,

**Applications** The CB amplifier is not commonly used for amplification purpose. It is used for

- matching a very low impedance source
- as a non-inverting amplifier with voltage gain exceeding unity
- for driving a high impedance load
- as a constant current source

**Characteristics of Common Emitter Amplifier**

- The current gain $A_i$ is high for $R_L$(<10KΩ)
- The Voltage gain is high for normal values of load resistance $R_L$,
- The input resistance $R_i$ is medium, and
- The output resistance $R_o$ is moderately high.

**Applications** Of the three configurations CE amplifier alone is capable of providing both voltage gain and current gain. Further the input resistance Ri and the output resistance Ro are moderately high. Hence CE amplifier is widely used for amplification purpose.

**Characteristics of Common Collector Amplifier**

- For low value of $R_L$ (<10KΩ) the current gain $A_i$ is high and almost equal to that of a CE amplifier,
- The voltage gain $A_v$ is less than unity,
- The input resistance is the highest of all the three configurations, and
- The output resistance is the lowest of all the three configurations
-

**Applications** The CC amplifier is widely used as a buffer stage between a high Impedance source and a low impedance load. The CC amplifier is called the Emitter Follower:

**FET SMALL SIGNAL MODEL:-**

The ac analysis of a FET configuration requires that a small signal ac model for the FET be developed.

The gate – to – source voltage controls the drain – to – source (channel) current of an FET.through a relationship known as Shockley's equation:

$$I_D = I_{DSS}(1 - V_{GS}/V_p)^2$$

The change in collector current that will result from a change in gate – to – source voltage can be determined using the transconductance factor $g_m$ : $\Delta I_D = g_m \Delta V_{GS}$



Solving for $g_m$ we have :

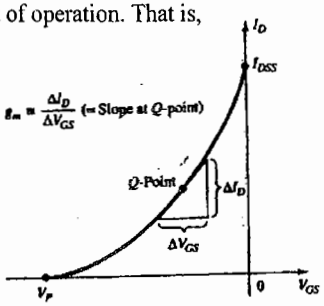
$$g_m = \Delta I_D / \Delta V_{GS}$$

$g_m$ is actually the slope of the transfer characteristics at the point of operation. That is,

$$g_m = m = \Delta y / \Delta x = \Delta I_D / \Delta V_{GS}$$

The slope, and therefore $g_m$, increase as we progress from $V_p$ to $I_{DSS}$. Or, in other words, as $V_{GS}$ approaches 0V, the magnitude of $g_m$ increases.

An alternative approach to determine $g_m$ employs the fact that the derivative of a function at a point is equal to the slope of the tangent line drawn at that point.




$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}\bigg|_{Q\text{-pt}} = \frac{d I_D}{d V_{GS}}\bigg|_{Q\text{-pt}} = \frac{d}{d V_{GS}} [I_{DSS}(1 - V_{GS}/V_p)^2]$$

$$= I_{DSS} \frac{d}{d V_{GS}} (1 - \frac{V_{GS}}{V_P})^2$$

$$= 2 I_{DSS} [1 - \frac{V_{GS}}{V_P}] \frac{d}{d V_{GS}} (1 - \frac{V_{GS}}{V_P})$$

$$= 2 I_{DSS} [1 - \frac{V_{GS}}{V_P}] \frac{d}{d V_{GS}} (1) - \frac{1}{V_P} \cdot \frac{d V_{GS}}{d V_{GS}}$$

$$= 2 I_{DSS} [1 - \frac{V_{GS}}{V_P}] [0 - \frac{1}{V_P}]$$

and $$g_m = \frac{2 I_{DSS}}{|V_P|} [1 - \frac{V_{GS}}{V_P}]$$

where $|V_p|$ denotes magnitude only to ensure a positive value for $g_m$.

Maximum value of $g_m$ for JFET in which $I_{DSS}$ and $V_p$ are specified is $g_m = \frac{2I_{DSS}}{|V_p|}\left(1 - \frac{0}{V_p}\right)$

$$g_{m0} = \frac{2 I_{DSS}}{|V_P|}$$

$$g_m = g_{m0}\left(1 - \frac{V_{GS}}{V_p}\right)$$

A mathematical relationship between $g_m$ and the dc bias current $I_D$ can be derived by noting that Shockley's equation can be written in the following form :

$$1 - \frac{V_{GS}}{V_P} = \sqrt{\frac{I_D}{I_{DSS}}}$$

$$\therefore g_m = g_{m0}(1 - \frac{V_{GS}}{V_P}) = g_{m0} \sqrt{\frac{I_D}{I_{DSS}}}$$

Note if $I_D = I_{DSS}$ , $g_m = g_{m0}$

$$I_D = \frac{I_{DSS}}{2} \quad , \quad g_m = 0.707\, g_{m0}$$

$$I_D = \frac{I_{DSS}}{4}, \quad g_m = 0.5\, g_{m0}$$

Input Impedance $Z_i \rightarrow$ The input impedance of all commercially available FETs is sufficiently large to assume that the input terminals approximate an open circuit. In equation form,

$$Z_i\,(FET) = \infty\ \Omega$$

Output impedance $Z_0 \rightarrow$

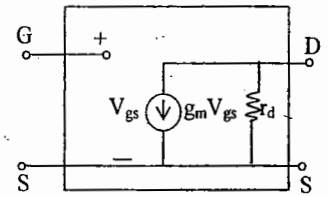
$$Z_0\,(FET) = r_d = \frac{\Delta V_{DS}}{\Delta I_D}\Bigg|_{V_{GS}\ =\ constant}$$

The output impedance is defined on the characteristics as the slope of the horizontal characteristic curve at the point of operation.

FET AC Equivalent Circuit →

The control of $I_D$ by $V_{GS}$ is included as a current source $g_m V_{gs}$ connected from drain to source. The current source has its arrow pointing from drain to source to establish a 180° phase shift between output and input voltages.

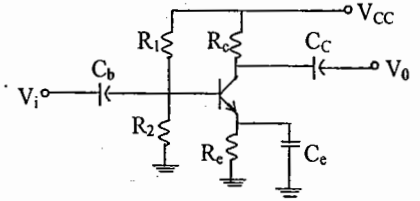
The input impedance is represented by the open circuit at the input terminals and the output impedance by the resistor $r_d$ from drain to source. Note that the gate to source voltage is now represented by $V_{gs}$ to distinguish it from dc levels. The source is common to both input and output circuits while the gate and drain terminals are only in "touch" through the controlled current source $g_m V_{gs}$.




## OBJECTIVES SET - A

1. In the transistor amplifier shown in the figure, the ratio of small signal voltage gain when the emitter resistor $R_e$ is bypassed by the capacitor $C_e$ to when it is not bypassed, (assuming simplified approximate h – parameter model for transistor, is

a) 1
b) $h_{fe}$
c) $\frac{(1 + h_{fe})\, R_e}{h_{ie}}$
d) $1 + \frac{(1+h_{fe})\, R_e}{h_{ie}}$



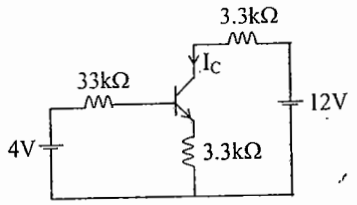

2. One of the applications of current mirror is

a) output current limiting
b) obtaining a very high current gain
c) current feed back
d) temperature stabilized biasing



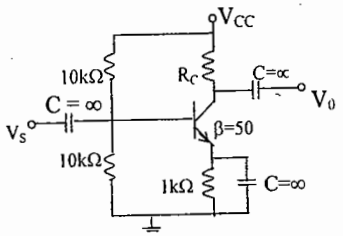
3. In the circuit, assume that the transistor has $h_{FE} = 99$ and $V_{BE} = 0.7$ V. The value of collector current $I_C$ of the transistor is approximately

a) [3.3 / 3.3] mA
b) [3.3 / (3.3 + 0.33)] mA
c) [3.3 / 33] mA
d) [3.3 / (33 + 3.3)] mA



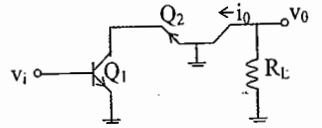

4. The transconductance $g_m$ of the transistor shown is 10 mS. The value of the input resistance $R_{in}$ is

a) 10.0 kΩ
b) 8.3 kΩ
c) 5.0 kΩ
d) 2.5 kΩ




5. In the CASCODE amplifier, if the common emitter stage ($Q_1$) has a transconductance $g_{m1}$, and the common base stage ($Q_2$) has a transconductance $g_{m2}$, then the overall transconductance is

a) $g_{m1}$
b) $g_{m2}$
c) $g_{m1}/2$
d) $g_{m2}/2$

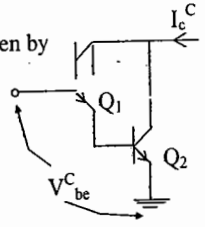



6. The $f_T$ of a BJT is related to its $g_m$, $C_\pi$ and $C_\mu$ as follows :

a) $f_T = \frac{C_\pi + C_\mu}{g_m}$ b) $f_T = \frac{2\pi(C_\pi + C_\mu)}{g_m}$ c) $f_T = \frac{g_m}{C_\pi + C_\mu}$ d) $f_T = \frac{g_m}{2\pi(C_\mu + C_\pi)}$

7. A Darlington stage is shown. If the transconductance of $Q_1$ is $g_{m1}$ and $Q_2$ is $g_{m2}$, then the overall transconductance $g_{mc} = \left(\frac{\Delta I_c^C}{\Delta V_{be}^C}\right)$ is given by

a) $g_{m1}$
b) 0.5 $g_{m1}$
c) $g_{m2}$
d) 0.5 $g_{m2}$



8. For a bipolar transistor, $h_{oe}$ has the dimensions of
(a) 0hms, (b) Siemens, (c) Amperes, (d) mhos,

9. The common-emitter leakage current of a bipolar transistor is high, if

(a) the temperature is high, (b) the temperature is low,
(c) $V_{CE}$ is high, (d) $h_{re}$ is high, (e) the frequency is high.

10. The h-parameter model is more commonly used because

(a) the h-parameters can be measured more accurately,
(b) the h-parameters do not vary with frequency,
(c) the analysis, using the h-parameters, gives the same expressions for the performance measures for all the configurations,
(d) the h-parameter model is an accurate representation of the transistor mechanism.

11. The potential divider bias is more commonly used because it

(a) uses minimum circuit components.
(b) uses only one battery,
(c) does not reduce the input and output impedances drastically,
(d) stabilises the collector current.

12. The common collector circuit has a voltage gain which is

(a) much higher than unity, (b) equal to unity,
(c) slightly less than unity, (d) far less than unity.

13. The circuit, having the lowest input impedance, is

(a) a C-E circuit, (b) a C-B circuit, (c) a C-C circuit, (d) none of the above.

14. The approximate C-E h-parameter model can be used for analysis when

(a) $h_{re}$ is very small (b) $h_{oe}$ is very small
(c) $R_L$ is very small (d) $h_{re}$ and (hoe $R_L$ are very small)

15. In an R-C coupled amplifier, if the emitter by-pass capacitor $C_e$ is disconnected, the mid-band gain of the stage will

(a) increase (b) decrease (c) remain unchanged (d) become unstable



16. The common-base stage is not used for a cascaded chain AF amplifiers because of its
(a) low input resistance (b) low-current gain
(c) high-output resistance (d) zero phase-shift for the signal

17. In an R-C coupled amplifier, the low frequency response will be improved by
(a) decreasing the value of the coupling capacitor
(b) increasing the value of the coupling capacitor
(c) removing the coupling capacitor
(d) none of the above.

18. The short-circuit current gain-bandwidth product of a transistor changes with change in

(a) the configuration (b) the operating collector current
(c) the value of load impedance (d) the value af source impedance

**Key- SET A**

**1. 2.d 3.b 4.c 5.a 6.d 7.a 8.b 9.a 10.d 11.d 12.b**

**13.b 14.d 15.b 16.a 17.c 18.b**

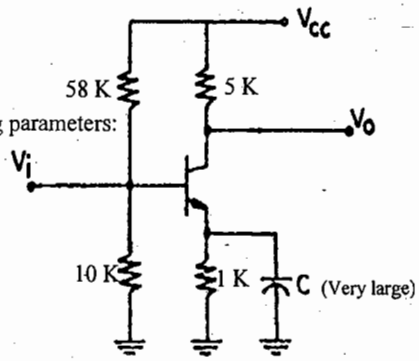
## SET - B

01. Choose the correct match for input resistance of various amplifier configurations shown below

| Configuration | Input resistance |
|---|---|
| CB: Common Base | LO: Low |
| CC: Common Collector | MO: Moderate |
| CE: Common emitter | HI: High |

(A) CB – LO, CC – MO, CE – HI
(B) CB – LO, CC – H I, CE – MO
(C) CB – MO, CC – H I, CE – LO
D) CB – H I, CC – LO, CE – MO

02. The transistor in the amplifier shown has following parameters:
$h_{fe} = 100$, $h_{ie} = 2\ K\Omega$, $h_{re} = 0$, $h_{oe} = 0.5$ m mhos,
The output impedance is
(A) 20 KΩ (B) 16 KΩ
(C) 5 KΩ (D) 4 KΩ




03. The configuration of a CASCODE amplifiers is

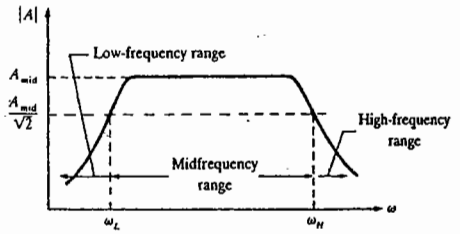
(A) CE – CE (B) CE – CB (C) CC – CB (D) CC - CC

**KEY:** (1) B (2) D (3) B

## Chapter: 4 FREQUENCY RESPONSE

The frequency of the applied signal can have a pronounced effect on the response of a single or multistage network. At low frequencies we shall find that the coupling and bypass capacitors can no longer be replaced by the short circuit approximation because of the increase in reactance of these elements. The frequency-dependent parameters of the small signal equivalent circuits and the stray capacitive elements associated with the active device and the network will limit the high-frequency response of the system. An increase in the number of stages of a cascaded system will also limit both the high and low-frequency responses.

For the RC coupled amplifiers the drop at low frequencies is due to the increasing reactance of $C_C$, $C_S$, or $C_E$, while its upper frequency limit is determined by either the parasitic capacitive elements of the network and frequency dependence of the gain of the active device. For the direct coupled amplifier, there are no coupling or bypass capacitors to cause a drop in gain at low frequencies. As the figure indicates, it is a flat response to the upper cutoff frequency which is determined by either the parasitic capacitances of the circuit or the frequency dependence of the gain of the active device.




There is a band of frequencies in which the magnitude of the gain is either equal or relatively close to the mid band value. To fix the frequency boundaries of relatively high gain, 0.707 $A_{Vmid}$ is chosen to be the gain at the cutoff levels. The corresponding frequencies ($f_L$) and ($f_H$) are generally called the corner, cutoff, break, or half power frequencies. The multiplier 0.707 was chosen because at this level the output power is half the mid band power output, that is, at mid frequencies,

$$P_{0\,mid} = \frac{|V_0^2|}{R_0} = \frac{|A_{Vmid}\,V_i|^2}{R_0}$$

and at the half – power frequencies,

$$P_{0\,HPF} = \frac{|0.707A_{Vmid}\,V_i|^2}{R_0} = 0.5\,\frac{|A_{Vmid}V_i|^2}{R_0}$$

and $P_{0\,HPF} = 0.5\,P_{0\,mid}$

The band width of each system is determined by $f_1$ and $f_2$,

$$\text{Band width} = BW = f_2 - f_1$$

A decibel plot can be obtained by applying

$$\left|\frac{A_V}{A_{Vmid}}\right|_{dB} = 20\log_{10}\frac{A_V}{A_{Vmid}}$$



It should be understood that most amplifiers introduce a 180° phase shift between input and output signals only in the midband region. At low frequencies there is a phase shift such that $V_0$ lags $V_i$ by an increased angle. At high frequencies the phase shift will drop below 180°.

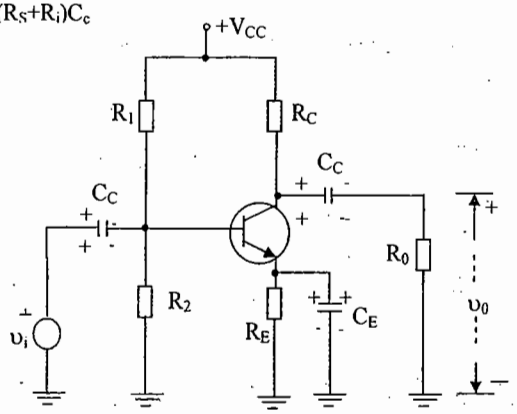
### *Low Frequency Response – BJT Amplifier*

The analysis here will employ the loaded voltage – divider BJT bias configuration, but the results can be applied to any BJT configuration. For the following network, the capacitors $C_S$, $C_C$ and $C_E$ will determine the low frequency response.

***$C_c$*** : Since $C_c$ is normally connected between the applied source and the active device, the general form of the RC configuration is established by the following network.

The total resistance is now $R_S + R_i$ and the cut off frequency is

$$f_{Ls} = \frac{1}{2\pi(R_S+R_i)C_c}$$




At mid-or high frequencies the reactance of the capacitor will be sufficiently small to permit a short circuit approximation for the element. The voltage $V_i$ will then be related to $V_s$ by

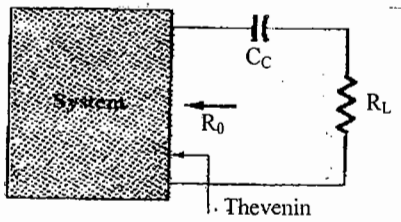
$$V_i\Big|_{mid} = \frac{R_i\,V_S}{R_i + R_S}$$

At $f_{Ls}$ the voltage $V_i$ will be 70.7% of the value determined by above equation assuming that $C_c$ is the only capacitive element controlling the low frequency response.

The voltage $V_i$ applied to the input of the active device can be calculated using the voltage-divider Rule:

$$V_i = \frac{R_i\,V_S}{R_S + R_i - jX_{Cc}}$$

***$C_C$*** : Since the coupling capacitor is normally connected between the output of the active device and the applied load, the R-C configuration that determines the low cutoff frequency due to $C_C$ appears as shown

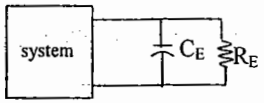


The total series resistance is now $R_0 + R_L$ and the cutoff frequency due to $C_C$ is determined by

$$f_{LC} = \frac{1}{2\pi(R_0+R_L)C_c}$$

Ignoring the effects of $C_S$ and $C_E$, the output voltage $V_0$ will be 70.7% of its mid band value at $f_{LC}$. Where $R_0 = R_d || r_0$

***$C_E$*** : To determine $f_{LE}$ the network "seen" by $C_E$ must be determined




Once the level of $R_e$ is established, the cutoff frequency due to $C_E$ can be determined using the following

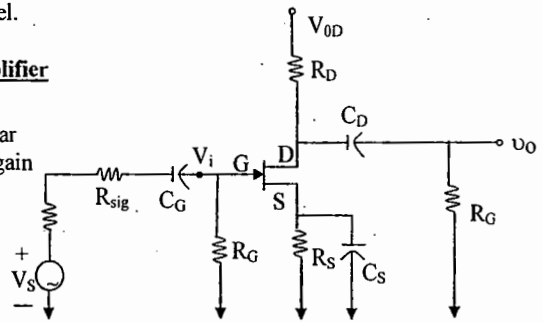
equation: $f_{LE} = \frac{1}{2\pi R_e C_E}$

At $f_{LE}$ the gain will be 3db below the mid band value determined with $R_E$ "shorted out".

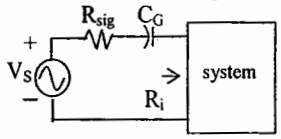
Although each will affect the gain $A_V = V_0/V_i$ in a similar frequency range, the highest low frequency cut off determined by $C_S$, $C_C$ or $C_E$ will have the greatest impact since it will be the last encountered before the midband level.

**Low Frequency Response – FET Amplifier**

The analysis of the FET amplifier in the low-frequency region will be quite similar to that of the BJT amplifier. There are again three capacitors of primary concern: $C_G$, $C_C$ and $C_S$.




***$C_G$*: For the coupling capacitor** between the source and the active device the ac equivalent network is as shown




The cutoff frequeney determined by $C_G$ will then be

$$f_{LG} = \frac{1}{2\pi(R_{sig}+R_i)C_G} \quad \text{Also } R_i = R_G$$

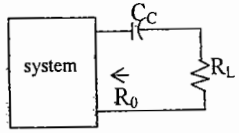
Typically, $R_G >> R_{sig}$ and the lower cutoff frequency will be determined primarily by $R_G$ and $C_G$. The fact that $R_G$ is so large permits a relatively low level of $C_G$ while maintaing a low cutoff frequency level for $f_{LG}$.



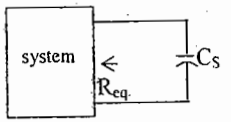
***$C_C$*: For the coupling capacitor** between the active device and the load the network is as shown:

The resulting cutoff frequency is

$$f_{LC} = \frac{1}{2\pi(R_0+R_L)C_C}, \text{ where } R_0 = R_D || r_d$$




***$C_S$*: For the source capacitor $C_S$** The cutoff frequency is




$$f_{LS} = \frac{1}{2\pi R_{eq} C_S}$$

$$\text{Where, } R_{eq} = \frac{R_S}{1 + R_S\,[\,(1+g_m r_d)/(r_d + R_D || R_L)\,]}$$

Which for $r_d \cong \infty\ \Omega$ becomes

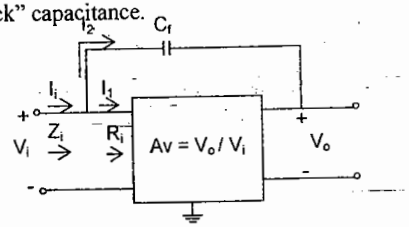
$$R_{eq} = \frac{R_S}{1 + R_S g_m} = R_S || \frac{1}{g_m}$$

***Miller Effect Capacitance →***

In the high frequency region the capacitive elements of importance are the inter electrode (between terminals) capacitances internal to the active device and the wiring capacitance between leads of the network. The large capacitors of the network that controlled the low-frequency response have all been replaced by their short-circuit equivalent due to their very low reactance levels.

For inverting amplifiers (phase shift of 180° between input and output resulting in a negative value for $A_V$) the input and output capacitances are increased by a capacitance level sensitive to the inter electrode capacitance between the input and output terminals of the device $C_f$ and the gain of the amplifier. $C_f$ is the "feedback" capacitance.

***Miller input capacitance →***

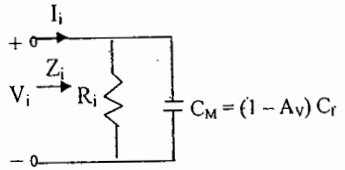



Applying KCL gives $I_i = I_1 + I_2$

Using ohm's law yields $I_i = \frac{V_i}{Z_i}$, $I_1 = \frac{V_i}{R_i}$,

and $I_2 = \frac{V_i - V_0}{X_{Cf}} = \frac{V_i - A_v V_i}{X_{Cf}} = \frac{(1-A_v)Vi}{X_{Cf}}$

Substituting, we obtain $\frac{V_i}{Z_i} = \frac{V_i}{R_i} + \frac{(1-A_v)Vi}{X_{Cf}}$




and $\frac{1}{Z_i} = \frac{1}{R_i} + \frac{1}{X_{Cf}/(1-A_v)}$

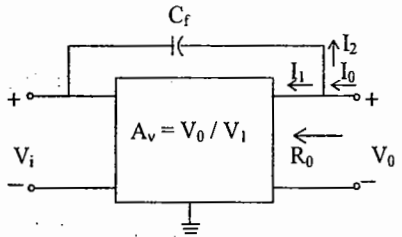
$$\underbrace{\frac{1}{\omega(1-A_V)\,C_f}}_{C_M} = X_{CM}$$

and $\frac{1}{Z_i} = \frac{1}{R_i} + \frac{1}{X_{cm}}$

In general, therefore, the Miller effect input capacitance is defined by: $C_{Mi} = (1-A_V)C_f$

For any inverting amplifier the input capacitance will be increased by Miller effect capacitance

***Miller output Capacitance →***




The Miller effect will also increase the level of output capacitance, which must also be considered when the high-frequency cutoff is determined. Applying KCL will result in

$$I_0 = I_1 + I_2$$

$$\text{With } I_1 = \frac{V_0}{R_0} \quad \text{and } I_2 = \frac{(V_0 - V_i)}{X_{Cf}}$$

The resistance $R_0$ is usually sufficiently large to permit ignoring the first term of the equation compared to the second term and assuming that

$$I_0 \cong \frac{(V_0 - V_i)}{X_{Cf}}$$

Substituting $V_i = V_0/A_v$ from $A_v = V_0/V_i$ will result in

$$I_0 = \frac{V_0 - V_0/A_V}{X_{Cf}} = \frac{V_0(1 - 1/A_V)}{X_{Cf}}$$

and $\frac{I_0}{V_0} = \frac{1 - 1/A_V}{X_{Cf}}$

(or) $$\frac{V_0}{I_0} = \frac{X_{Cf}}{1 - 1/A_V}$$

$$= \frac{1}{\omega_{Cf}(1 - 1/A_V)}$$

$$= \frac{1}{\omega C_{m\,o}}$$

resulting in the following equation for the Miller output capacitance: $C_{Mo} = (1 - 1/A_v)\, c_f$

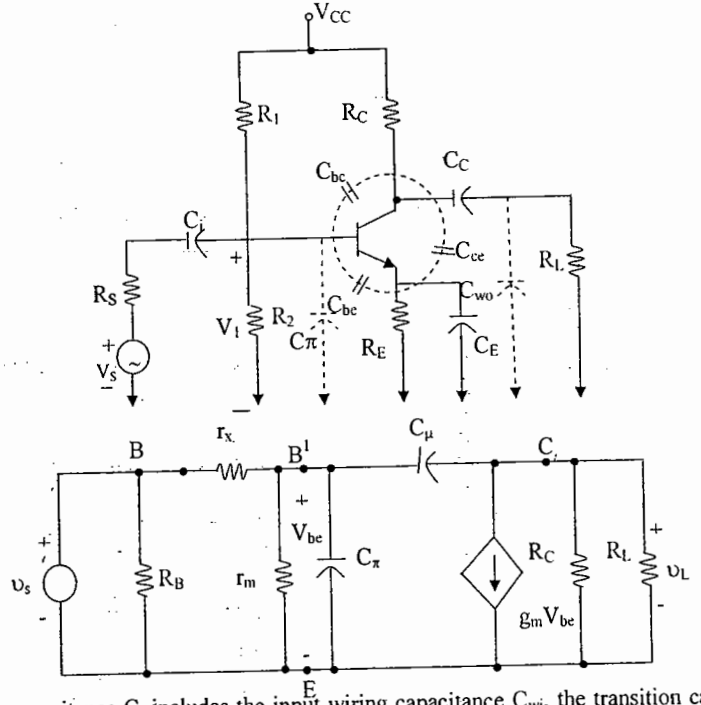
For the usual situation where $|A_v| >> 1$

$C_{Mo} \cong C_f$



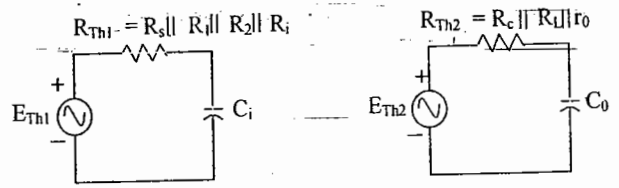
**High Frequency Response – BJT Amplifier →**

At the high-frequency end there are two factors that will define the –3dB point: the network capacitance (parasitic and introduced) and the frequency dependence of $h_{fe}(\beta)$.




The capacitance $C_i$ includes the input wiring capacitance $C_{wi}$, the transition capacitance $C_{bc}$ and the Miller capacitance $C_{Mi}$. The capacitance $C_0$ includes the output wiring capacitance $C_{wo}$, the parasitic capacitance $C_{ce}$, and the output Miller Capacitance $C_{Mo}$

The Thevenin equivalent circuit for the input and output networks are




For the network the –3dB frequency is defined by $f_{Hi} = \frac{1}{2\pi R_{Th1} C_i}$

with $R_{Th1} = R_s \| R_1 \| R_2 \| R_i$

and $C_i = C_{wi} + C_{be} + C_{Mi} = C_{wi} + C_{be} + (1\text{-}A_V)\, C_{be}$

At very high frequencies the effect of $C_i$ is to reduce the total impedance of the parallel combination of $R_1$, $R_2$, $R_i$ and $C_i$. The result is a reduced level of voltage across $C_i$, a reduction in $I_b$, and gain for the system.

For the output network, $f_{Ho} = \dfrac{1}{2\pi R_{Th2} C_0}$

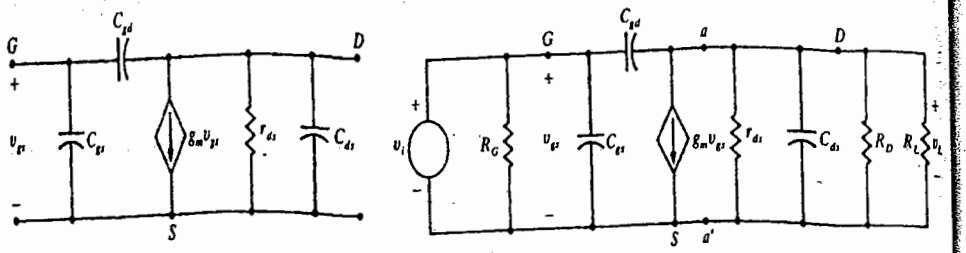
with $R_{Th2} = R_c \| R_L \| r_0$

and $C_0 = C_{wo} + C_{ce} + C_{Mo}$

At very high frequencies the capacitive reactance of $C_0$ will decrease and consequently reduce the total impedance of the output parallel branches.

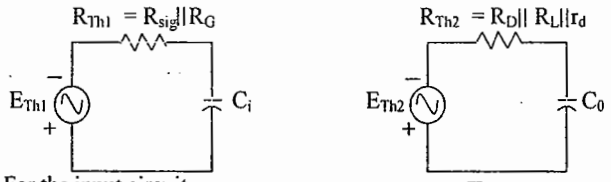
The frequencies $f_{Hi}$ and $f_{Ho}$ will each define a –6dB/octave asymptote. The lowest frequency would be the determining factor.

**High Frequency Response –FET Amplifier →**




At high frequencies $C_i$ will approach a short-circuit equivalent and $V_{gs}$ will drop in value and reduce the overall gain. At frequencies where the $C_0$ approaches its short circuit equivalent the parallel output voltage $V_0$ will drop in magnitude.

The cutoff frequencies defined by the input and output circuits can be obtained by first finding the Thevenin equivalent circuits.




For the input circuit,

$$f_{Hi} = \frac{1}{2\pi R_{Th1} C_i}$$

and $R_{Th1} = R_{sig} \| R_G$

with $C_i = C_{wi} + C_{gs} + C_{Mi}$

and $C_{Mi} = (1 - A_v) C_{gd}$

and for the output circuit,

$$f_{Ho} = \frac{1}{2\pi R_{Th2} C_0}$$

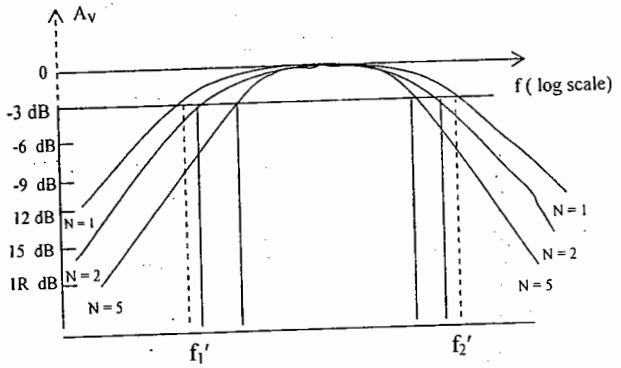
with $R_{Th2} = R_D \| R_L \| r_d$



and $C_0 = C_{wo} + C_{ds} + C_{Mo}$

and $C_{Mo} = \left(1 - \dfrac{1}{A_v}\right) C_{gd}$

**Multistage Frequency Effects**




For n stages

$A_{V\ low\ (overall)} = A_{V\ 1low} \times A_{V\ 2\ low} \times A_{V\ 3\ low} \ldots\ldots \times A_{V\ n\ low}$

$A_{V\ low(overall)} = (A_{V1\ low})^n$, for identical stages.

Or $\dfrac{A_{V1\ low\ (overall)}}{A_{Vmid}} = \left(\dfrac{A_{V1\ low}}{A_{Vmid1}}\right)^2 = \dfrac{1}{(1 - j\, f_1/f)^n}$

Setting the magnitude of this result equal to $\dfrac{1}{\sqrt{2}}$ (-3dB level) results in

$$f_1' = \frac{f_1}{\sqrt{2^{1/n} - 1}}$$

In a similar manner, it can be shown that for the high frequency region,

$$f_2' = \sqrt{(2^{1/n} - 1)}\ f_2$$

A decrease in bandwidth is not always associated with an increase in the number of stages if the midband gain can remain fixed and independent of the number of stages.

## OBJECTIVE QUESTIONS SET - A

1. Generally, the gain of a transistor amplifier falls at high frequencies due to the

a) internal capacitance of the device b) coupling capacitor at the input

c) skin effect d) coupling capacitor at the output

2. The current gain of a bipolar transistor drops at high frequencies because of

a) transistor capacitances b) high current effects in the base

c) parasitic inductive elements d) the Early effect

3. A multistage amplifier has a low pass response with three real poles at s =-$\omega_1$, -$\omega_2$ and -$\omega_3$. The approximate overall bandwidth 'B' of the amplifier will be given by

a) $B = \omega_1 + \omega_2 + \omega_3$ b) $1/B = 1/\omega_1 + 1/\omega_2 + 1/\omega_3$

c) $B = (\omega_1 + \omega_2 + \omega_3)^{1/3}$ d) $B = \sqrt{\omega_1^2 + \omega_2^2 + \omega_3^2}$

4. Which of the following components control the low frequency of the RC coupled amplifier?

1) wiring capacitance 2) parasitic capacitance of transistor

3) coupling capacitors 4) emitter by pass capacitance

select the correct answer using the codes given below:

a) 1 and 2 b) 2 and 3 c) 3 an 4 d) 1,2 and 4

5. The CE current gain – bandwidth product of a transistor ($f_T$) is defined as the frequency at which

a) Alpha of the transistor falls by 3 dB b) Beta of the transistor falls by 3dB

c) Beta of the transistor falls to unity d) Power gain of the transistor falls to unity

6. Consider the following statements in respect of the transistor R-C coupled amplifier:

1. The low frequency response is determined by the transistor junction capacitors.
2. The high frequency response is limited by coupling capacitors
3. The Miller capacitance reduces the gain at high frequencies
4. As the gain is increased the bandwidth gets reduced.

Which of these statements are correct?

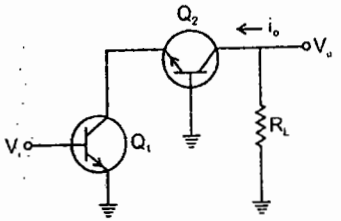
a) 1 and 2 b) 2 and 3 c) 3 and 4 d) 1 and 4

**KEY SET A: 1.a 2.a 3.a 4.c 5.c 6.c**



## SET - B

01. In the cascode amplifier shown in the figure, if the common – emitter stage ($Q_1$) has a transconductance $g_{m1}$, and the common base stage ($Q_2$) has a transconduc – tance $g_{m2}$, then the overall transconductance of the cascode amplifier is




(A) $g_{m1}$ (B) $g_{m2}$ (C) $\frac{G_{m1}}{2}$ (D) $\frac{G_{m2}}{2}$

02. An npn transistor (with C = 0.3 pF)has a unity – gain cutoff frequency $f_T$ of 400 MHz at a dc bias current $I_C$ = 1 mA. The value of its $C_\mu$ (in pF) is approximately ($V_T$ = 26 m V)

(A) 15 (B) 30 (C) 50 (D) 96

03. An amplifier is assumed to have a single-pole high-frequency transfer function.The rise time of its output response to a step function input is 35 nsec. The upper -3 dB frequency (in MHz) for the amplifier to a sinusoidal input is approximately

(A) 4.55 (B) 10 (C) 20 (D) 28.6

04. The current gain of the bipolar transistor drops at high frequencies because of

(A) transistor capacitances

(B) high current effects in the base

(C) parasitic inductive elements

(D) the Early effect

05. The current gain of BJT is

(A) $g_m r_o$ (B) $\frac{g_m}{r_o}$

(C) $g_m r_\pi$ (D) $\frac{g_m}{r_\pi}$

06. An npn BJT has $g_m$ = 38mA / V, $C_\mu = 10^{-14}$F, $C_\pi = 4 \times 10^{-13}$F, and DC current gain $\beta_0$ = 90. For this transistor $f_T$ and $f_\beta$ are

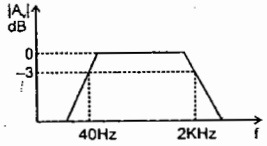
(A) $f_T = 1.64 \times 10^8$ Hz and $f_\beta = 1.47 \times 10^{10}$ Hz

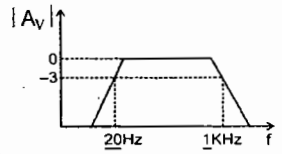
(B) $f_T = 1.47 \times 10^{10}$ Hz and $f_\beta = 1.64 \times 10^8$ Hz

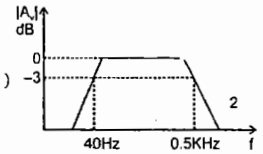
(C) $f_T = 1.33 \times 10^{12}$ Hz and $f_\beta = 1.47 \times 10^{10}$ Hz

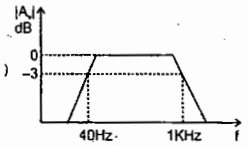
(D) $f_T = 1.47 \times 10^{10}$ Hz and $f_\beta = 1.33 \times 10^{12}$ Hz

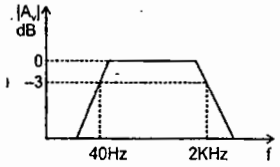
07. Three identical RC – coupled transistor amplifiers are cascaded. If each of the amplifiers has a frequency response as shown in the figure, the overall frequency response is as given in




(A)



(B)



(C)



(D)



08. Generally, the gain of a transistor amplifier falls at high frequencies due to the
(A) internal capacitances of the device
(B) coupling capacitor at the input
(C) skin effect
(D) coupling capacitor at the output

09. Three identical amplifiers with each one having a voltage gain of 50, input resistance of 1 KΩ and output resistance of 250 Ω, are cascaded. The open circuit voltage gain of the combined amplifier is
(A) 49 dB (B) 51 dB
(C) 98 dB (D) 102 dB

10. A bipolar transistor is operating in the active region with a collector current of 1mA. Assuming that the β of the transistor is 100 and the thermal voltage ($V_T$) is 25mV, the transconductance ($g_m$) and the input resistance ($r_\pi$) of the transistor in the common emitter configuration, are
(A) $g_m = 25mA / V$ and $r_\pi = 15.625\ k\Omega$
(B) $g_m = 40mA / V$ and $r_\pi = 4.0\ k\Omega$
(C) $g_m = 25mA / V$ and $r_\pi = 2.5\ k\Omega$
(D) $g_m = 40mA / V$ and $r_\pi = 2.5\ k\Omega$

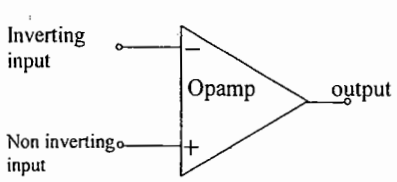
11. The cascode amplifier is a two stage configuration of
(A) CC – CB (B) CE – CB
(C) CB – CC (D) CE – CC

**KEY: SET B**

(1) A (2) A (3) B (4) A (5) C
(6) B (7) A (8) A (9) C (10) D
(11) B



An operation amplifier is a very high gain amplifier having very high input impedance and low output impedance. The basic circuit is made using a difference amplifier having two inputs (plus and minus) and at least one output.



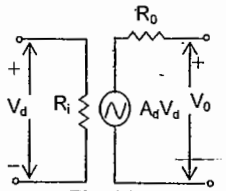



Fig. (a)

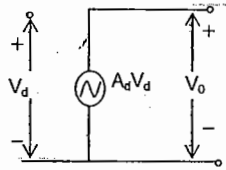


Fig. (b)

A plus (+) input produces an output that is in phase with the signal applied, while an input to the minus(-) input results in an opposite polarity output. The ac equivalent circuit of the op-amp is shown .The signal applied between input terminals sees an input impedance, $R_i$, typically very high. The output voltage is shown to be the amplifier gain times the input signal taken through the output impedance, $R_0$, which is typically very low.
An ideal op amp circuit would have infinite input impedance, zero output impedance, and an infinite voltage gain.

**Basic Op-Amp**
(with $R_1$ & $R_f$)

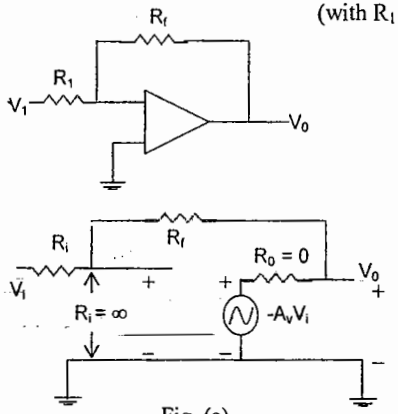


Fig. (a)

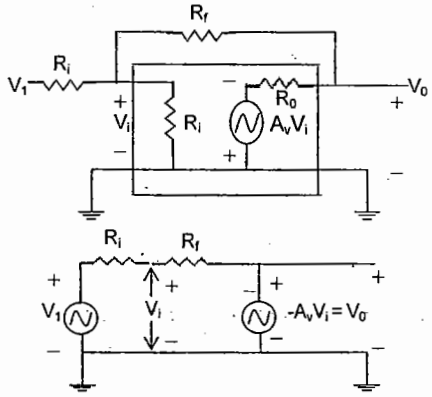


Fig. (b)

The circuit shown provides operation as a constant-gain multiplier. An input signal, $V_1$, is applied through resistor $R_1$ to the minus input. The output is then connected back to the same minus input through resistor $R_f$. The plus input is connected to ground. Since the signal $V_1$ is essentially applied to the minus input, the resulting output is opposite in phase to the input signal.If we use the ideal op-amp equivalent circuit, replacing $R_i$ by an infinite resistance and $R_0$ by zero resistance, the ac equivalent circuit is shown in fig(b). The circuit is then redrawn, from which circuit analysis is carried out.

$$V_i = \frac{R_f \quad V_1}{R_f + (1 + A_V)R_1}$$ If $A_V >> 1$ and $A_v R_1 >> R_f$, as is usually true, then $V_i = \frac{R_f}{A_v R_1} V_1$

$$V_0 = -A_v V_i \quad , \quad \frac{V_0}{V_i} = -\frac{R_f}{R_1}$$

***Unity gain***: If $R_f = R_1$, $V_0 / V_1 = -1$, so that the circuit provides a unity voltage gain with 180° phase inversion.

Constant Magnitude Gain: If $R_f$ is some multiple of $R_1$, the overall amplifier gain is a constant. If we select, precise resistor values for $R_f$ and $R_1$, we can obtain a wide range of gains, the gain being as accurate as the resistors used and is only slightly affected by temperature and other circuit factors.

Virtual Ground: The fact that $V_i \approx 0V$ leads to the concept that at the amplifier input there exists a virtual short circuit or virtual ground. The concept of a virtual short implies that although the voltage is nearly 0V, there is no current through the amplifier input to ground. Current only goes through resistors $R_1$ and $R_f$.

**Differential and common mode operation**

One of the important features of a differential circuit connection, as provided in an op-amp, is the circuit's ability to greatly amplify signals that are opposite at the two inputs, while only slightly amplifying signals that are common to both inputs.

Differential Inputs: when separate inputs are applied to the op-amp, the resulting difference signal is the difference between the two inputs.

$$V_d = V_{i1} - V_{i2}$$

***Common Inputs***: When both input signals are the same a common signal element due to the two inputs can be defined as the average of the sum of the two signals.

$$V_c = 1/2\ (V_{i1} + V_{i2})$$

***Output Voltage***: Since any signals applied to an op-amp in general have both in-phase and out of phase components, the resulting output can be expressed as

$$V_0 = A_d V_d + A_c V_c$$

Where

$V_d$ = difference voltage
$V_c$ = common voltage
$A_d$ = differential gain of the amplifier
$A_c$ = common-mode gain of the amplifier

Opposite polarity inputs: If opposite polarity inputs applied to an op-amp are ideally opposite signals,

$$V_{i1} = -V_{i2} = V_S, \quad V_d = V_{i1} - V_{i2} = V_s - (-V_s) = 2V_s$$

$$V_c = 1/2\ (V_{i1} + V_{i2}) = 1/2\ [V_s + (-V_s)] = 0$$

$$V_0 = A_d V_d + A_c V_c = A_d (2V_s) + 0 = 2A_d V_s$$

This shows that when the inputs are ideal opposite signals (no common element), the output is the differential gain times twice the input signal applied to one of the inputs.

Same Polarity Inputs: If the same polarity inputs are applied to an op-amp, $V_{i1} = V_{i2} = V_s$, $V_d = V_{i1} - V_{i2} = V_s - V_s = 0$, $V_C = 1/2\ (V_{i1} + V_{i2}) = 1/2\ (V_s + V_s) = V_s$

$$V_0 = A_d V_d + A_c V_c = A_d (0) + A_c V_s = A_c V_s$$

This shows that when the inputs are ideal in-phase signals (no difference signal), the output is the common-mode gain times the input signal, $V_s$, which shows that only common-mode operation, occurs.



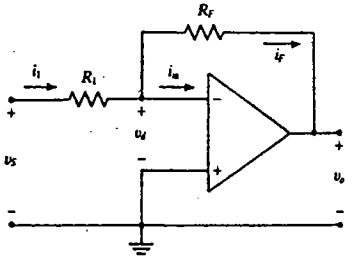
***Common-Mode Rejection Ratio***: $\text{CMRR} = \frac{A_d}{A_c}$, $\text{CMRR (log)} = 20 \log_{10} \frac{A_d}{A_c}$

It should be clear that the desired operation will have $A_d$ very large with $A_c$ very small. That is, the signal components of opposite polarity will appear greatly amplified at the output, whereas the signal components that are in phase will mostly cancel out so that the common mode gain, $A_c$, is very small. Ideally, the value of the CMRR is infinite. Practically, the larger the value of CMRR, the better the circuit operation.

$$V_0 = A_d V_d + A_c V_c = A_d V_d \left(1 + \frac{A_c V_c}{A_d V_d}\right) = A_d V_d \left(1 + \frac{1}{\text{CMRR}} \frac{V_c}{V_d}\right)$$

## PRACTICAL OP-AMP CIRCUITS

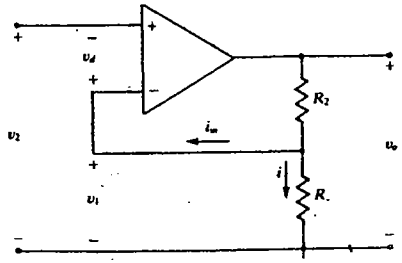
***Inverting Amplifier***:




The output is obtained by multiplying the input by a fixed or constant gain, set by the input resistor ($R_1$) and feedback resistor ($R_f$) – this output also being inverted from the input.

$$v_0 = \frac{-R_f}{R_i} v_s$$

***Non-inverting Amplifier***:

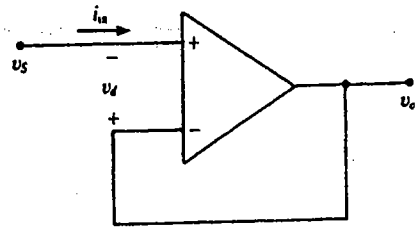



It should be noted that the inverting amplifier connection is more widely used because it has better frequency stability.

$$v_1 = \frac{R_1}{R_1 + R_2} v_0$$

$$\frac{v_0}{v_1} = \frac{R_1 + R_2}{R_1} = 1 + \frac{R_2}{R_1}$$

***Unity follower***:

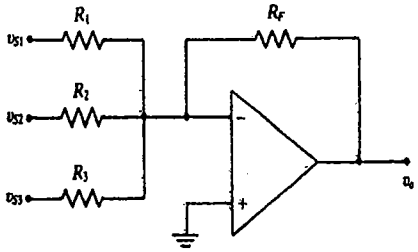



The unity-follower circuit, provides a gain of unity(1) with no polarity or phase reversal.

$$v_0 = v_S$$

and the output is of the same polarity and magnitude as the input.

***Summing Amplifier***:

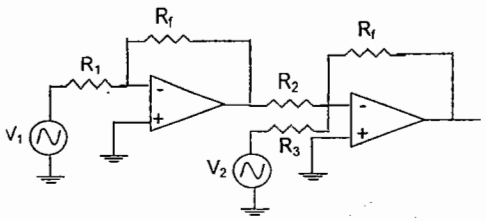



The circuit shows a three-input summing amplifier, which provides a means of algebraically summing (adding) three voltages, each multiplied by a constant-gain factor.

$$v_0 = \left(-\frac{R_f}{R_1} v_{s1} + \frac{R_f}{R_2} v_{s2} + \frac{R_f}{R_3} v_{s3}\right)$$

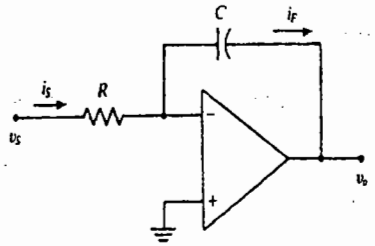
In other words, each input adds a voltage to the output multiplied by its separate constant-gain multiplier.

***Voltage Subtraction***:




$$V_0 = -\left(\frac{R_f}{R_2}V_2 - \frac{R_f}{R_3}\frac{R_f}{R_1}V_1\right)$$

## *Integrator*:




If the feedback component used is a capacitor, the resulting connection is called an integrator.

$$X_C = \frac{1}{j\omega C} = \frac{1}{sC}, \quad \frac{V_0}{V_S} = \frac{-1}{sCR}$$

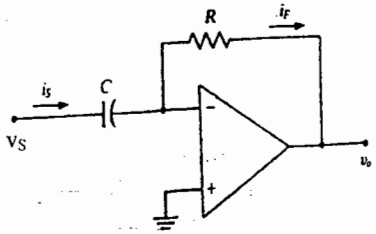
$$v_0(t) = -\frac{1}{RC}\int v_s(t)\,dt$$

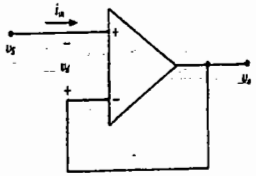
More than one input may be applied to an integrator with the resulting operation given by

$$v_0(t) = -\left(\frac{1}{R_1C}\int v_1(t)\,dt + \frac{1}{R_2C}\int v_2(t)\,dt + \frac{1}{R_3C}\int v_3(t)\,dt\right)$$

***Differentiator*** :

$$v_0(t) = -RC\frac{dv_S}{dt}(t)$$




***Voltage Buffer***:

$$v_0 = v_s$$

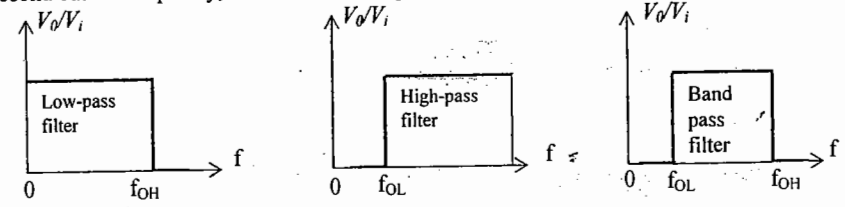
A voltage buffer circuit provides a means of isolating an input signal from a load by using a stage having unity voltage gain, with no phase or polarity inversion, and acting as an ideal circuit with very high input impedance and low output impedance.

## ACTIVE FILTERS

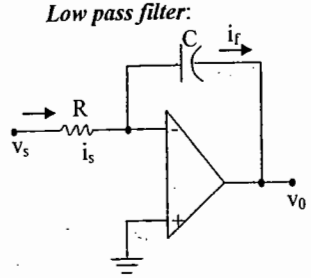
A filter circuit can be constructed using passive components: resistors and capacitors. An active filter additionally uses an amplifier to provide voltage amplification and signal isolation or buffering.

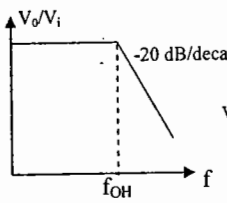


A filter that provides a constant output from dc upto a cutoff frequency $f_{OH}$ and then passes no signal above that frequency is called an ideal low-pass filter.
A filter that provides or passes signals above a cut off frequency $f_{OL}$ is a high pass filter.
When the filter circuit passes signals that are above one ideal cut off frequency and below a second cut off frequency, it is called a band pass filter.



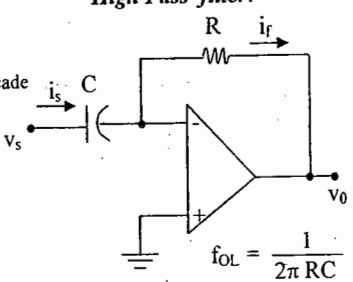

***Low pass filter***:



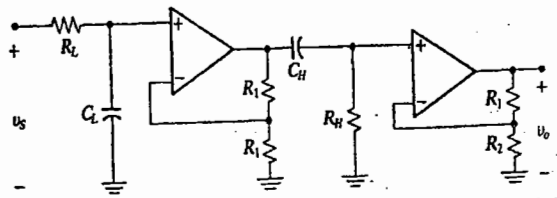

$$f_{OH} = \frac{1}{2\pi RC}$$

***High Pass filter***:




$$f_{OL} = \frac{1}{2\pi RC}$$

***Band pass filter***:

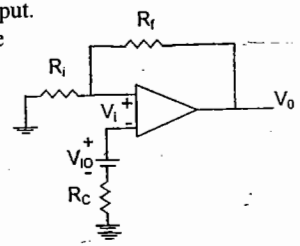



The figure shows a band pass filter using two stages, the first a high pass filter and the second a low pass filter, the combined operation being the desired band pass response.

$$f_{OL} = \frac{1}{2\pi R_L C_L} \qquad f_{OH} = \frac{1}{2\pi R_H C_H}$$

## OP AMP SPECIFICATIONS

Offset currents and Voltages: While the Op-amp output should be 0V when the input is 0V, in actual operation there is some offset voltage at the output. The output offset voltage can be affected by two separate circuit conditions. These are : 1) an input offset voltage, $V_{IO}$ and 2) an offset current due to the difference in currents resulting at the plus (+) and minus(-) inputs.



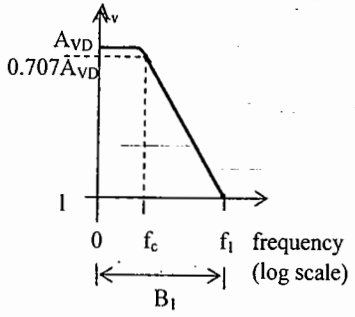

$$V_{0(offset)} = V_{IO}\frac{R_i + R_f}{R_i}$$
$$V_{0(offset)} = I_{IO}R_f$$

***Input Bias current, $I_{IB}$:***

A parameter related to $I_{IO}$ and the separate input bias currents $I^+_{IB}$ and $I^-_{IB}$ is the average bias current defined as

$$I_{IB} = \frac{I^+_{IB} + I^-_{IB}}{2}, \quad I^+_{IB} > I^-_{IB}, \quad I^+_{IB} = I_{IB} + \frac{I_{IO}}{2}, \quad I^-_{IB} = I_{IB} - \frac{I_{IO}}{2}$$

***Gain Band width***: Because of the internal compensation circuits included in an op amp, the voltage gain drops off as frequency increases.
A frequency of interest is where the gain drops by 3dB, this being the cutoff frequency of the op-amp, $f_C$. The unity gain frequency $f_t$ and cutoff frequency are related by $f_t = A_{VD} f_C$ = gain × BW where $A_{VD}$ is differential voltage gain.
Slew Rate, SR is maximum rate at which amplifier output can change in volts per μs.




$$SR = \frac{\Delta V_0}{\Delta t} \text{ V/μs}$$

***Maximum Signal Frequency***: Let $V_0 = K \sin 2\pi ft$
The maximum voltage rate of change can be shown to be signal maximum rate of change = $2\pi fK$ V/s. To prevent distortion at the output the rate of change must also be less than the slew rate, i.e,

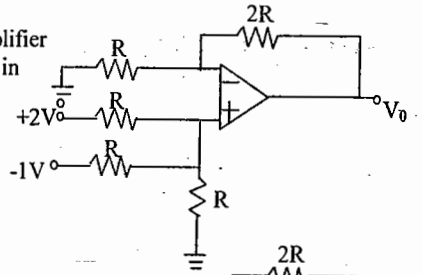
$$2\pi fK \le SR \qquad \omega \le \frac{SR}{K} \text{ rad / sec}$$

***OBJECTIVES SET – A***

1. An ideal OPAMP is used to make an inverting amplifier. The two input terminals of the OPAMP are at the same potential because
   a) the two input terminals are directly shorted internally
   b) the input impedance of the OPAMP is infinity
   c) the open loop gain of the OPAMP is infinity
   d) CMRR is infinity

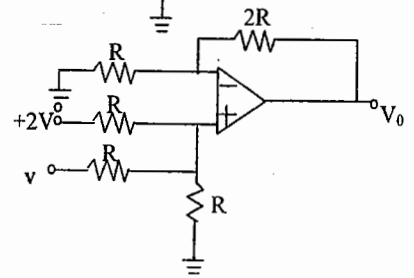
2. An analog comparator is a high-gain amplifier whose output is always either positive or in negative saturation. TRUE / FALSE

3. Figure shows a non inverting op-amp summer. $V_0$ = .....




5. A non inverting op-Amp is shown. $V_0$ is equal to

   a)(3/2) Sin (100 t) b) 3 Sin (100t)
   c) 2 Sin (100t) d) None of the above

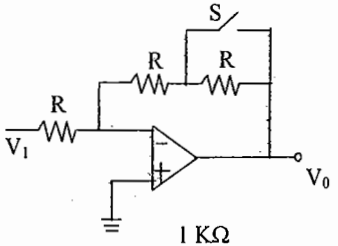



v = ( 2 + Sin 100t )V

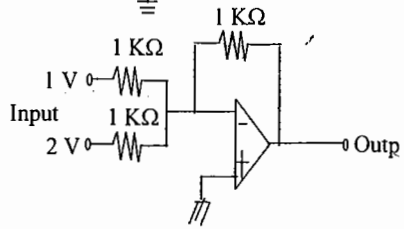


6. Let the magnitude of the gain in the inverting OP-Amp amplifier circuit shown in fig be x with switch S open. When the switch S is closed, the magnitude of gain becomes

   (a) x/2 (b) –x (c) 2x (d) –2x




8. The circuit shown in figure acts as a ____ . For the given inputs, its output voltage is___.

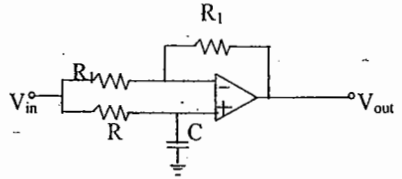



9. An op – amp has an open loop gain of $10^5$ and an open loop upper cutoff frequency of 10Hz. If this op – amp is connected as an amplifier with a closed loop gain of 100, then the new upper cutoff frequency is
   a) 10 HZ b) 100 HZ c) 10 KHZ d) 100 KHz

10. An op-amp, having a slew rate of 62.8 V/μ sec, is connected in a voltage follower configuration. If the maximum amplitude of the input sinusoidal is 10V, then the minimum frequency at which the slew rate limited distortion would set in at the output is
    a) 1.0 MHz b) 6.28 MHz c) 10.0 MHz d) 62.8 MHz.

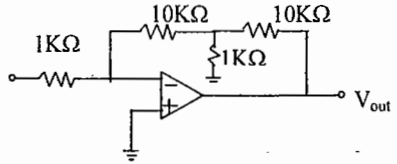
11. For the circuit of figure with an ideal operational amplifier, the maximum phase shift of the output $V_{out}$ with reference to the input $V_{in}$ is

    a) 0°
    b) -90°
    c) +90°
    d) ± 180°



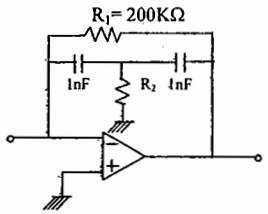

12. Assuming the op-Amp to be ideal, the gain $V_{out} / V_{in}$ in the circuit shown is

    a) –1
    b) –20
    c) –100
    d) –120




13. In the active filter circuit shown if Q=1, a pair of poles will be realized with $\omega_0$ equal to

    a) 1000 rad/s
    b) 100 rad/s
    c) 10 rad/s
    d) 1 rad / s



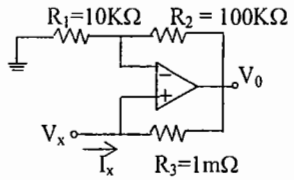
14. The input resistance $R_{IN}$ ( $=V_x/I_x$) of the circuit is

a) +100 KΩ

b) –100 KΩ

c) +1 MΩ

d) –1MΩ




15. If the differential voltage gain and the common mode voltage gain of a differential amplifier are 48dB and 2dB respectively, then its common mode rejection ratio is
a) 23 dB b) 25 dB c) 46 dB d) 50 dB

16. A 741-type op-Amp has a gain-band width product of 1MHz. A non inverting amplifier using this op-Amp and having a voltage gain of 20dB will exhibit a –3dB bandwidth of
a) 50 KHz b) 100 KHz c) 1000/17 KHz d) 1000/7.07 KHz

17. An amplifier using an op Amp with a slew rate SR = 1 V/μ sec has a gain of 40 dB. If this amplifier has to faithfully amplify sinusoidal signals from dc to 20 KHz without introducing any slew rate induced distortion, then the input signal level must not exceed
a) 795 mV b) 395 mV c) 79.5 mV d) 39.5 mV

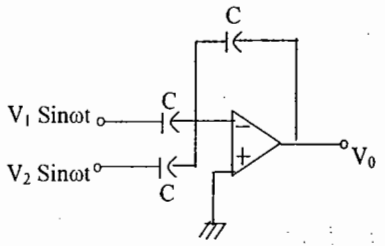
18. If the op – amp is ideal, then $V_0$ is

a) zero

b) $(V_1 - V_2)$ Sin ωt

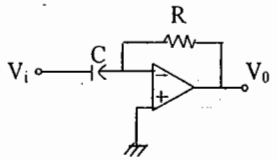
c) $-(V_1 + V_2)$ Sin ωt

d) $(V_1 + V_2)$ Sin ωt




19. Assume that the op – amp is ideal. If $V_i$ is a triangular wave, the $V_0$ will be

a) square wave
b) triangular wave
c) parabolic wave
d) sine wave




***KEY:***

1. c, d 2. true 3.1V 4. $V_0$ 5. b 6. c 7. c 8. summer, –3V

9. c 10.a 11.d 12.d 13.a 14.b 15.c 16.b 17.c 18. c 19. a



## SET – B

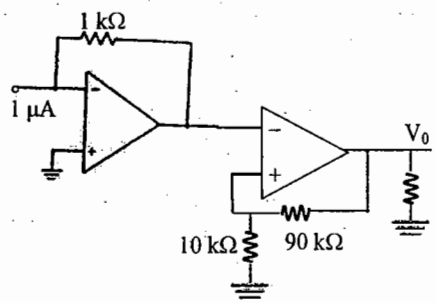
01. In a single-stage differential amplifier, the output offset voltage is basically dependent on the mismatch of

(a) $V_{BE}$, $I_B$ and β (b) $V_{BE}$ and $I_B$
(c) $I_B$ and β (d) $V_{BE}$ and β

02. A second –order band-pass active filter can be obtained by cascading a low-pass second order section having cutoff frequency $f_{OH}$ with a high-pass second- order section having cut off frequency $f_{OL}$, provided

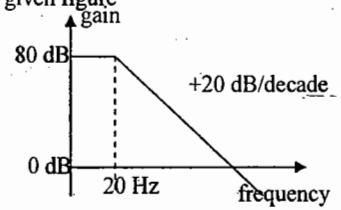
(a) $f_{OH} > f_{OL}$ (b) $f_{OH} < f_{OL}$
(c) $f_{OH} = f_{OL}$ (d) $f_{OH} \leq f_{OL}$

03. The output voltage $V_0$ of the given circuit is



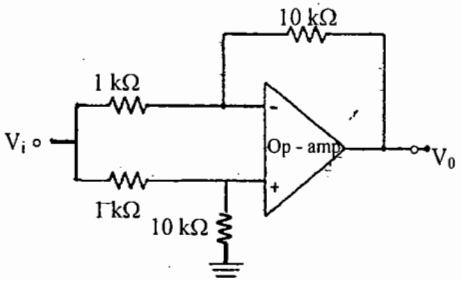

(a)-100 V (b)-100 mV
(c)10 V (d)-10 mV

04. The voltage gain verses frequency curve of an Op-Amp is shown in the given figure




The gain-bandwidth product of the Op-Amp is
(a) 200 Hz (b) 200 MHz
(c) 200 kHz (d) 2 MHz

05. The $V_0$ of the Op-Amp circuit shown in the given figure is




(a) 11 $V_i$ (b) 10 $V_i$
(c) $V_i$ (d) 0

06. Consider the following statements:
A totem pole configuration used in the output stage of an Op-Amp has the advantage of using

1. only n-p-n BJTs
2. complimentary symmetrical pair of transistors
3. only one transistor

Which of these statements is/ are correct?
(a) 1 alone (b) 2 alone
(c) 3 alone (d) 1 and 3

07. A 1 ms pulse can be stretched to 1 Sec pulse by using

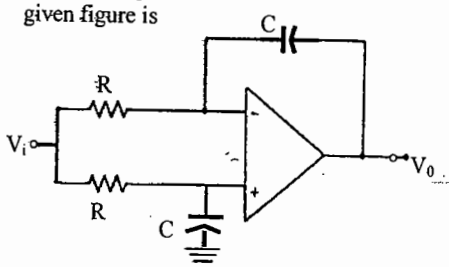
(a) an astable multivibrator

(b) a monostable multivibrator

(c) a bistable multivibrator

(d) a Schmitt trigger circuit

08. The Op-Amp circuit shown in the given figure is



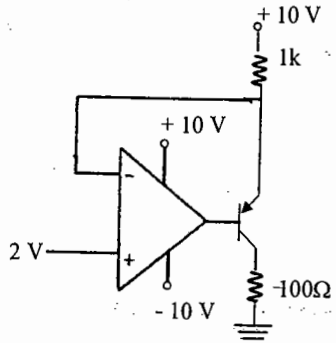

(a) a high-pass circuit

(b) a low-pass circuit

(c) a band-pass circuit

(d) an all-pass circuit

09. In the circuit shown in the given figure, the current flowing through resistance of 100 Ω would be




(a) 8 mA (b) 10 mA
(c) 20 mA (d) 100 mA

10. In a 741 Op-Amp, there is 20 dB/decade fall-off starting at a relatively low frequency. This is due to the

(a) applied load

(b) internal compensation

(c) impedance of the source

(d) power dissipation in the chip

11. The input differential stage Op-Amp 741 is biased at about 10 μA current. Such a low current of the input stage gives

(a) high CMRR

(b) high differential gain

(c) low differential gain

(d) high input impedance

Which of these are correct?

(a) 1 and 2 (b) 1,2 and 4

(c) 3 and 4 (d) 1,2,3 and 4

12. In a circuit, if the open loop gain is $10^6$ and output voltage is 10 volt, the differential voltage should be

(a) 10 μV (b) 0.1 V
(c) 100 μV (d) 1 μV

13. An operational amplifier possesses

(a) very large input resistance and very large output resistance
(b) very small input resistance and very small output resistance
(c) very large input resistance and very small output resistance
(d) very small input resistance and very output

14. Consider the following statements:
In order to generate square wave from a sinusoidal input signal one can use

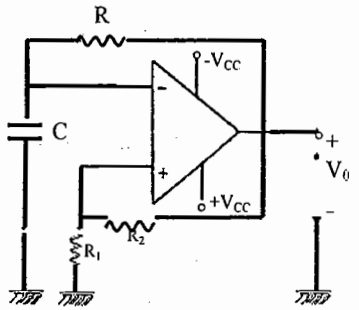
1. Schmitt trigger circuit
2. Clippers and amplifiers
3. Monostable multivibrators

Which of the above statements is/are correct?

(a) 1 along (b) 1 and 2
(c) 2 and 3 (d) 1,2 and 3



15. An op-amp circuit is shown in the figure
The output $V_0$ will be (assume ideal op-amp)



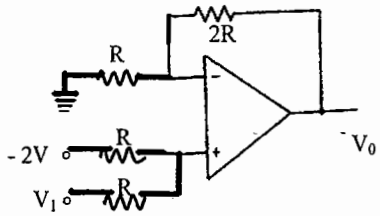

(a) equal to zero because the input is zero

(b) dependent on element values, hence nothing can be predicted without a knowledge of element values

(c) a square wave varying between $+V_{CC}$ and $-V_{CC}$

(d) a sinusoidal wave of amplifier $V_{CC}$

16. A non-inverting op-amp is shown (assume ideal op-amp)
The output voltage $V_0$, for an input $V_1 = [2 + \sin(100t)]V$ is




$V_1 = [2 + \sin(100\,t)]$

(a) 3/2 sin (100 t) (b) 3 sin (100 t)

(c) 2 sin (100 t) (d) 3 sin (100 t) + ½

17. Match List-I (Circuit Name) with List-II (Characteristics) and select the correct answer using the codes given below the lists:

List-I
A. Schmitt trigger
B. Monostable multivibrator
C. Astable multivibrator
D. Blocking oscillator

List-II
1. It needs a pulse transformer
2. it is used to generate gating pulse whose width can be controllee
3. it is bistable circuit
4. it has no stable state

**Codes:**

| | A | B | C | D |
|---|---|---|---|---|
| (a) | 3 | 2 | 4 | 1 |
| (b) | 2 | 3 | 1 | 4 |
| (c) | 3 | 2 | 1 | 4 |
| (d) | 2 | 3 | 4 | 1 |

18. A triangular – square wave generator uses

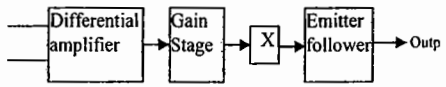
(a) A sine wave oscillator and a comparator

(b) An integrator and a comparator

(c) A differentiator and a comparator

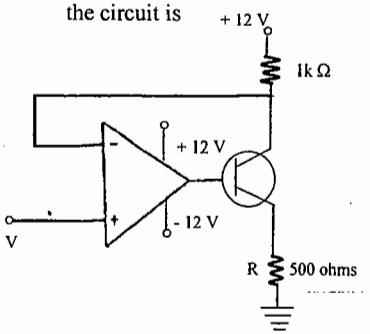
(d) A sine wave oscillator and a clipper

19. The stage marked X in the architecture of a two-stage op-amp is



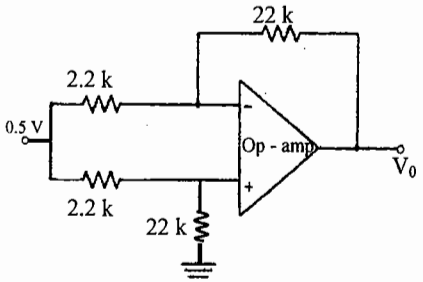

(a) Direct coupled amplifier
(b) Buffer amplifier
(c) Level shifter
(d) Blocking osciliator

20. The current through the resistor R in the circuit is



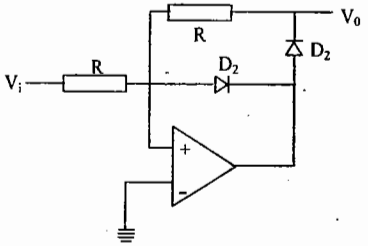

(a) 1 mA (b) 4 mA
(c) 8 mA (d) 10 mA

21. In the op-amp circuit shown (assuming ideal op-amp), $V_0$ is



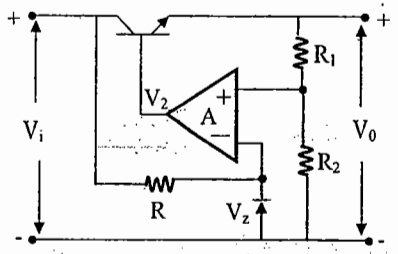

(a) $V_0 = -5V$ (b) $V_0 = +5V$
(c) $V_0 = 0$ (d) $V_0 = -2V$

22. Consider the following circuit:



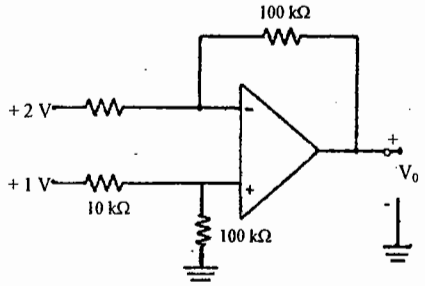

What is the function of diode $D_2$ in the above circuit?
(a) To avoid saturation of the Op-Amp
(b) To provide negative feedback when the input is negative
(c) To reduce reverse breakdown voltage of $D_1$
(d) As a buffer

23. Consider the following circuit:



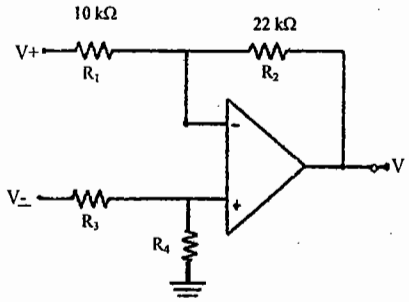

Which one of the following expressions for $V_0$ is correct?
(a) $V_0 = V_Z$ (b) $V_0 = AV_2$
(c) $V_0 = AV_Z$ (d) $V_0 = -AV_Z$

24. Consider the following Op-Amp circuit: $V_0$ is equal to




(a) +10 V (b) -10 V
(c) + 11 V (d) -11 V

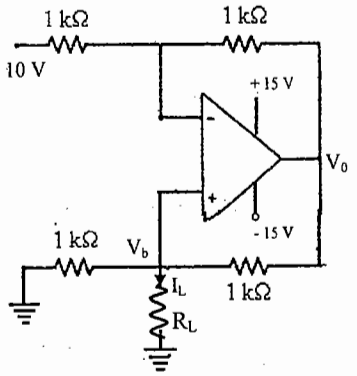
25. Consider the following circuit:




What is the value of $R_4$ in the above circuit, if the voltage $V_-$ and $V_+$ are to be amplified by the same amplification factor?
(a) 7 kΩ (b) 22 kΩ
(c) 33 kΩ (d) 35 kΩ

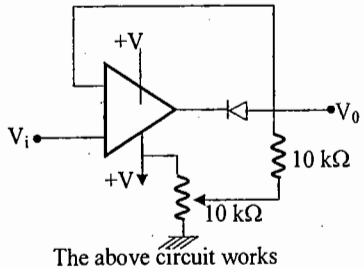


26. The load current $I_L$ in the circuit shown is



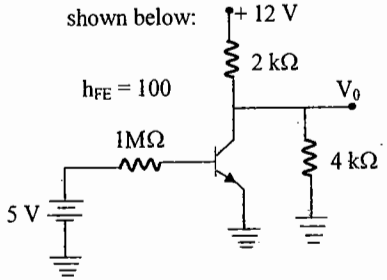

(a) – 5 mA (b) – 10 mA
(c) + 25 mA (d) + 50 mA

27. Consider the following circuit:




The above circuit works
(a) As a logarithmic amplifier
(b) As a negative clipper
(c) As a positive clipper
(d) As a half-wave rectifier

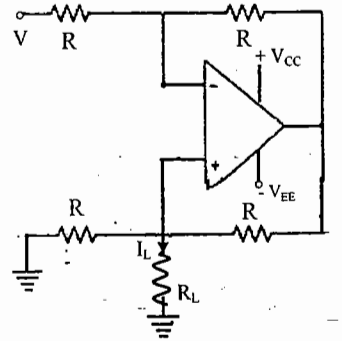
28. Consider the NPN transistor circuit shown below:




The output voltage $V_0$ in the circuit is
(a) 0 V (b) 12 V
(c) 9 V (d) 5 V

29. Pulses of definite width can be obtained from regular shaped pulses:
(a) when it is given as input to a monostable multivibrator
(b) when it is given as triggering signal to a bistable multivibrator
(c) when it is used as input to a Schmitt trigger
(d) when it is used as input to a pulse transformer

30. For the circuit given below, what is $I_L$ equal to?

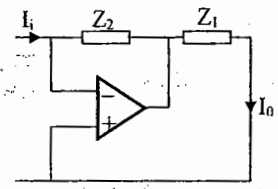



(a) $V/R_L$ (b) $V/R$
(c) $\frac{V}{R+R_L}$ (d) $\frac{V}{2R+R_L}$

31. For a given op-amp, CMRR=$10^5$ and differential gain = $10^5$. What is the common mode gain of the op-amp?

(a) $10^{10}$ (b) $2X10^5$
(c) $10^5$ (d) 1

32. In the circuit shown the transfer function $I_0/I_i$ is




(a) $-Z_2/Z_1$ (b) $-Z_1/Z_2$ (c) $1+(Z_2/Z_1)$ (d) $1+(Z_1/Z_2)$

33. Narrow pulses with adjustable mark to space ratio can be obtained form square wave input signal by using
1. Schmitt trigger
2. Monostable multivibrator
3. Clippers

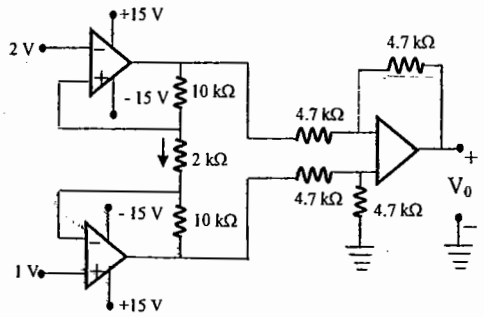
Select the correct answer using the code given below:

(a) only 1 (b) only 2
(c) 1 and 2 (d) 2 and 3

34. A differential amplifier has inputs, $V_1 = 1050\ \mu V$ and $V_2 = 950\ \mu V$ with CMRR = 1000. The error in the differential output is

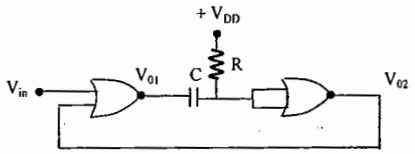
(a) 10% (b) 1%
(c) 0.1% (d) 0.01%

35. The output voltage $V_o$ of the circuit is



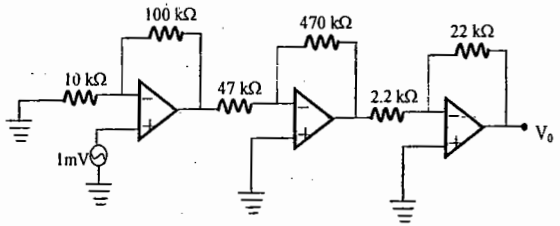

(a) -11 V (b) 6 V (c) 11 V (d) -6 V

36. The figure given shows the circuit of




(a) Bi-Stable multivibrator
(b) Schmitt trigger
(c) Monostable multivibrator
(d) Astable multivibrator

37. The output voltage $V_o$ of the below circuit is




(a) -1.1 V (b) +1.1 V
(c) 1.0 V (d) 10 V

38. Consider the following statements: Dominant-pole frequency compensation in an OP-AMP

1. Increases the slow-rate of the OP-AMP
2. increases the stability of the OP-AMP
3. reduces the bandwidth of the OP-AMP
4. reduces the CMRR of the OP-AMP

Which of the statements given above are correct?

(a) 1 and 3 only (b) 1,2 and 4
(c) 1 and 2 only (d) 2 and 3 only



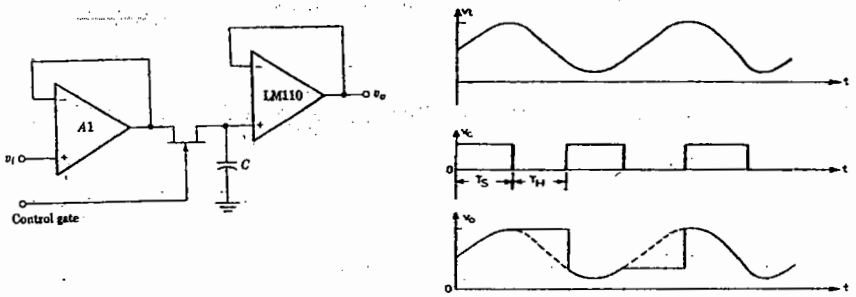
**KEY: SET B**

| | | | | | |
|---|---|---|---|---|---|
| (01) C | (02) A | (03) D | (04) C | (05) D | (06) A |
| (07) B | (08)B | (09) A | (10) B | (11) B | (12) A |
| (13) B | (14) A | (15) A | (16) A | (17) A | (18) B |
| (19) C | (20) D | (21) C | (22) B | (23) C | (24) B |
| (25) C | (26) B | (27) C | (28) A | (29) C | (30) B |
| (31) D | (32) A | (33) B | (34) B | (35) A | (36) C |
| (37) B | (38) C | | | | |

## Sample and Hold Circuit, Schmitt Trigger & Multivibrators

### *SAMPLE AND HOLD CIRCUIT →*

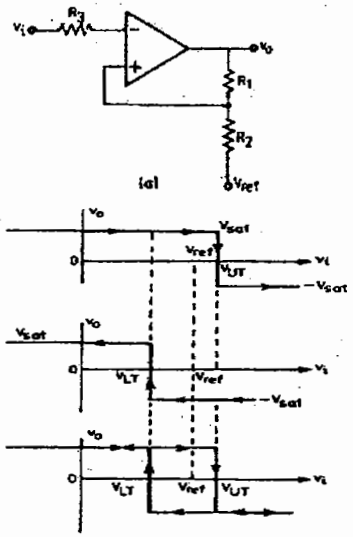
A sample and hold circuit samples an input signal and holds on to its last sampled value until the input is sampled again.




The n – channel E – MOSFET works as a switch and is controlled by the control voltage $V_C$ and the capacitor C stores the charge. The analog signal $V_i$ to be sampled is applied to the drain of E – MOSFET and the control voltage $v_i$ is applied to its gate. When $v_i$ is positive, the E – MOSFET turns on and the capacitor C charges to the instantaneous value of input $v_i$ with a time constant $[(R_0 + r_{DS}(on)]$ C. Here $R_0$ is the output resistance of the voltage follower $A_1$ and $r_{DS}(on)$ is the resistance of the MOSFET when on. Thus the input voltage $v_i$ appears across the capacitor C and then at the output through the voltage follower $A_2$.
During the time when control voltage $v_i$ is zero, the E – MOSFET is off. The capacitor C is now facing the high input impedance of the voltage follower $A_2$ and hence cannot discharge. The capacitor holds the voltage across it. The time period $T_S$, the time during which voltage across the capacitor is equal to input voltage is called sample period. The time period $T_H$ of $v_c$ during which the voltage across the capacitor is held constant is called hold period. The frequency of the control voltage should be kept higher than (at least twice) the input so as to retrieve the input from output wave form.

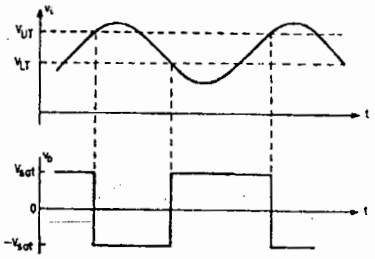
### *SCHMITT TRIGGER →*

This is also known as regenerative comparator. The input voltage is applied to the ( - ) input terminal and feed back voltage to the ( + ) input terminal. The input voltage $v_i$ triggers the output $v_0$ every time it exceeds certain voltage levels. These voltage levels are called upper threshold voltage ($V_{UT}$) and lower threshold voltage ($V_{LT}$). The hysteresis width is the difference between these two threshold voltages (i.e.,) $V_{UT} - V_{LT}$
These threshold voltages are calculated as follows
Suppose the output $v_0 = +v_{sat}$. The voltage at (+) input terminal will be $V_{ref} + \frac{R_2}{R_1 + R_2}(V_{sat} - V_{ref}) = V_{UT}$






As long as $V_i$ is less than $V_{UT}$, the output $v_0$ remains constant at $+V_{sat}$. When $v_i$ is just greater than $V_{UT}$, the output regeneratively switches to $-V_{sat}$ and remains at this level as long as $v_i > V_{UT}$.



For $v_0 = -V_{sat}$, the voltage at the (+) input terminal is,

$$V_{ref} - \frac{R_2 (V_{sat} + V_{ref})}{R_1 + R_2} = V_{LT}$$

The input voltage $V_i$ must become lesser than $V_{LT}$ in order to cause $v_0$ to switch from $-V_{sat}$ to $+V_{sat}$.
A regenerator transition takes place and the output $v_0$ returns from $-V_{sat}$ to $+V_{sat}$ almost instantaneously.

The most important application of schmitt trigger circuit is to convert a very slowly varying input voltage into a square wave output.

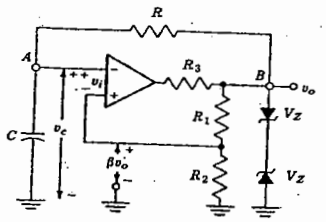
If in the circuit, $V_{ref}$ is chosen as zero volt,

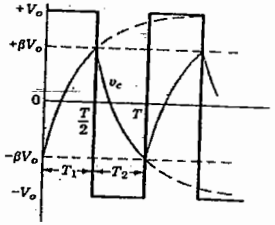
$$V_{UT} = -V_{LT} = \frac{R_2 V_{sat}}{R_1 + R_2}$$

If an input sinusoid of frequency f = 1/T is applied to such a comparator, a symmetrical square wave is obtained at the output.

### *MULTIVIBRATORS →*

#### *Astable Multivibrator*



A simple op – amp square wave generator, also called a free running oscillator, the principle of generation of square wave output is to force an op – amp to operate in the saturation region.

A fraction $\beta = \frac{R_2}{R_1 + R_2}$ of the output is fed back to the (+) input terminal. Thus the reference

voltage $V_{ref}$ is $\beta V_0$ and may take values as $+\beta V_{sat}$ or $-\beta V_{sat}$. The output is also fed back to the (-) input terminal after integrating by means of a low – pass RC combination. Whenever input at the (-) input terminal just exceeds $V_{ref}$, switching takes place resulting in a square wave output. In astable multi vibrator, both the states are quasi stable.

The frequency is determined by the time it takes the capacitor to charge from $-\beta V_{sat}$ to $+\beta V_{sat}$ and vice versa.

The voltage across the capacitor as a function of time is given by, $V_c(t) = V_f + (V_i - V_f)\, e^{-t/RC}$

Where, the final value, $V_f = +V_{sat}$ and the initial value, $V_i = -\beta V_{sat}$

Therefore,

$$V_C(t) = V_{sat} + (-\beta V_{sat} - V_{sat})\, e^{-t/RC}$$

Or $$V_C(t) = V_{sat} - V_{sat}(1 + \beta)\, e^{-t/RC}$$

At $t = T_1$, voltage across the capacitor reaches $\beta V_{sat}$ and switching takes place, therefore,

$$V_C(T_1) = \beta V_{sat} = V_{sat} - V_{sat}(1+\beta)e^{-T1/RC}$$

After algebraic manipulation , we get

$$T_1 = RC \ln \frac{(1+\beta)}{(1-\beta)}$$

This gives only one half of the period

Total time period

$$T = 2T_1 = 2RC \ln \frac{(1+\beta)}{(1-\beta)}$$ and the output waveform is symmetrical.

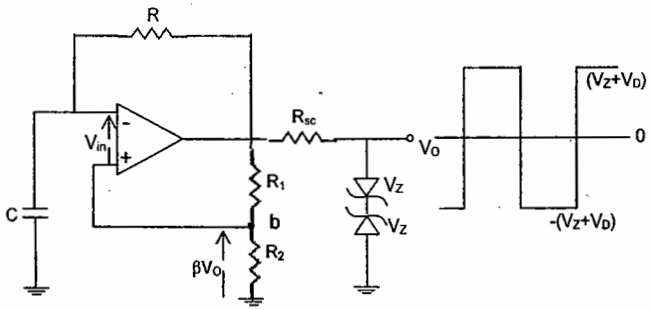
If $R_1 = R_2$, then $\beta = 0.5$ and $T = 2RC \ln 3$. And for $R_1 = 1.16R_2$. It can be seen that $T = 2RC$.

$$\text{Or } f_0 = \frac{1}{2RC}$$

The output swings from $+V_{Sat}$ to $-V_{sat}$, so,

$v_0$ peak – to – peak $= 2V_{sat}$

The peak to peak output amplitude can be varied by varying the power supply voltage. However, a better technique is to use back Zener diodes.






The output voltage is regulated to $\pm(v_z+v_0)$ by the zener diodes.

$v_0$ peak to peak $= (v_z + v_0)$

$$I_{SC} = \frac{v_{sat} - v_z}{R_{SC}}$$

If an asymmetric square wave is desired, then zener diodes with different breakdown voltages $v_{z1}$ and $v_{z2}$ may be used.

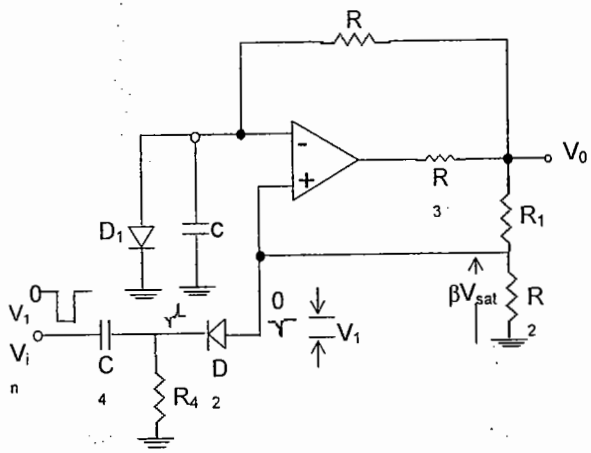
$V_{01} = v_{z1} + v_D$

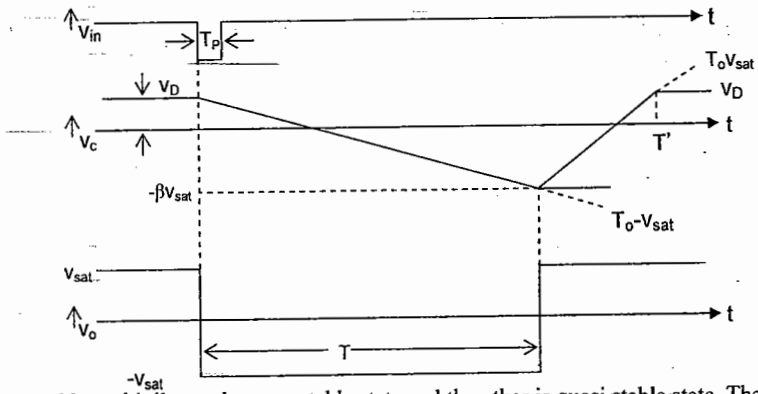
$V_{02} = v_{z2} + v_D$

$$T_1 = RC \ln \frac{1 + \beta\,(v_{02} / v_{01})}{1 - \beta}$$

An alternative method to get asymmetric square wave output is to add a dc voltage source v in series with $R_2$.

***MONOSTABLE MULTIVIBRATOR →***




Monostable multivibrator has one stable state and the other is quasi stable state. The circuit is useful for generating single output pulse of adjustable time duration in response to a triggering signal.

A diode $D_1$ clamps the capacitor voltage to 0.7v when the output is at $+v_{sat}$. A negative going pulse signal of magnitude $v_1$ passing through the differentiator $R_4C_4$ and diode $D_2$ produces a negative going trigerring impulse and is applied to the (+) input terminal.

The pulse width T of magnitude multivibrator is calculated as follows :
The general solution for a single time constant low pass RC current with $v_i$ and $v_f$ as initial and final values is, $v_0 = v_f + (v_i - v_f)\, e^{-t/RC}$

For the circuit, $v_f = -V_{sat}$ and $v_i = v_D$
The output $v_c$ is,

$$V_c = -v_{sat} + (v_D + v_{sat})e^{-t/RC}$$

At t = T

$$v_C = -\beta\, v_{sat}$$

therefore $-\beta\, v_{sat} = -v_{sat} + (v_D + v_{sat})\, e^{-t/RC}$
After simplification, pulse width T is obtained as

$$T = RC \ln \frac{(1 + v_D / v_{sat})}{1 - \beta}$$

where $\beta = \dfrac{R_2}{R_1 + R_2}$

If $v_{sat} >> v_D$ and $R_1 = R_2$ so that $\beta = 0.5$, then

$$T = 0.69\ RC$$

For monostable operation, the trigger pulse width $T_p$ should be much less than T, the pulse width of the monostable multivibrator.

The monostable multivibrator circuit is also referred to as time delay circuit as it generates a fast transition at a pre determined time t after the application of input trigger.

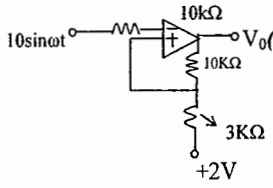
## OBJECTIVES QUESTIONS-

1. A sample and hold (S/H) circuit, having a holding capacitor of 0.1 nF, is used at the input of an ADC. The conversion time of the ADC is 1 μsec, and during this time, the capacitor should not lose more than 0.5% of the charge put across it during the sampling time. The maximum value of the input signal to the S/H circuit is 5V. The leakage current of the S/H circuit should be less than *(GATE'01, EEE)*

   a) 2.5 mA b) 0.25mA c) 25.0 μA d) 2.5 μA

2. The output voltage ($V_0$) of the Schmitt trigger shown in figure swings between +15V and –15V. Assume that the operational amplifier is ideal. The output will change from +15V to –15V. When the instantaneous value of the input sine wave is

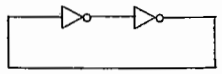
   a) 5V in the positive slope only
   b) 5V in the negative slope only
   c) 5V in the positive and negative slopes
   d) 3V in the positive and negative slopes



*(GATE'02, EEE)*

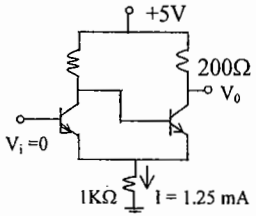


3. The digital circuit using two inverters will act as



   a) a bistable multivibrator
   b) an astable multivibrator
   c) a monostable multivibrator d) an oscillator *(GATE'04, EEE)*

4. In the Schmitt trigger circuit, if $V_{CE(sat)} = 0.1V$, the output logic low level ($V_{0L}$) is
   a) 1.25 V
   b) 1.35 V
   c) 2.50 V
   d) 5.00 V




5. Consider the following two statements : *(GATE'01, ECE)*
   Statement 1 : Astable multivibrator can be used for generating square wave.
   Statement 2 : Bistable multivibrator can be used for storing binary information.

   a) only statement 1 is correct b) only statement 2 is correct
   c) both the statements 1 and 2 are correct d) both the statements 1 and 2 are incorrect

6. The most commonly used amplifier in sample and hold circuits is *(GATE-2000, ECE)*
   a) a unity gain inverting amplifier b) a unity gain non – inverting amplifier
   c) an inverting amplifier with a gain of 10 d) an inverting amplifier with a gain of 100

7. Match List – I and List – II and select the correct answer using the codes given below the lists : *(IES-2003, ECE)*

   A. Schmitt trigger 1. It needs a pulse transformer
   B. Monostable multivibrator 2. It is used to generate getting pulse whose width can be controlled
   C. Astable multivibrator 3. It is a bistable circuit
   D. Blocking oscillator 4. It has no stable state

   a) A B C D: 3 2 4 1 b) A B C D: 2 3 1 4 c) A B C D: 3 2 1 4 d) A B C D: 2 3 4 1

8. A Schmitt trigger circuit is used for
   (a) shaping an input pulse into a square pulse, (b) producing a delayed pulse,
   (c) generating a ramp, (d) differentiating a pulse.

9. For producing an Identical delayed pulse, we should use a
   (a) bistable multivibrator, (b) astable multivibrator,
   (c) monos table multivibrator, (d) Schmitt trigger.

10. A Bootstrap Sweep uses a
    (a) common-emitter amplifier with a large voltage gain,
    (b) common-base amplifier with a large voltage gain,
    (c) common-collector amplifier with a large voltage gain close to unity,
    (d) high-gain narrow-band amplifier.

11. A Miller Sweep has a good linearity because it employs
(a) negative current feedback, (b) positive voltage feedback,
(c) negative voltage feedback, (d) compound feedback.

12. The speed-up capacitors are used in a bistable circuit in order to reduce
(a) the settling time, (b) the transition time,
(c) the trigger amplitude required, (d) the base biasing supply voltage.

13. In an ideal OPAMP, the input impedance RI and output impedance RQ are given by
(a) Ri=0, Ro= 0, (b) Ri=0 Ro= ∞, (c) Ri=∞,, Ro= ∞, (d) Ri=∞,, Ro= 0,.

14. Differential amplifiers are very commonly used in low-level d.c. amplifiers because of
(a) large bandwidth, (b) high input impedance,
(c) large-gain, (d) low offsets and drifts.

15. The frequency, at which the gain of an OPAMP is 0dB, is called
(a) cross-over frequency, (b) unity-gain cross-over frequency,
(c) take: off frequency, (d) zero dB frequency.

16. Frequency compensation has to be used in OPAMP's in order to
(a) increase the bandwidth, (b) increase the gain,
(c) improve the stability of gain, (d) decrease the drift.

17. The common-mode rejection ratio, of a BJT difference amplifier, can be Improved by
(a) increasing the emitter resistance, (b) increasing the collector resistance,
(c) decreasing the collector resistance, (d) decreasing the emitter resistance.

18. For square wave generation, _____ is used.
a) astable multivirator b) bistable multivibrator
c) monostable multivibrator d) none

19. For pulse wave generation, _____ is used.
a) astable multivirator b) bistable multivibrator
c) monostable multivibrator d) none

20. For flip-flop generation , _____ is used.
a) astable multivirator b) bistable multivibrator
c) monostable multivibrator d) none

21. The disadvantage of astable multivibrator is _____
a) it is used as a square wave generator
b) frequency can be changes by increasing the voltage
c) both the transistors may go into saturation simultaneously. d) None

22. Which of the following triggering is best suited for monostable multivibrator
a) symmetrical b) asymmetrical
c) symmetrical positive triggering d) symmetrical negative triggering



23. Purpose of collector catching diode in a binary is
a) to maintain constant o/p swing b) to maintain constant base saturation currents
c) both a & b d) none

24.Pulse width of a collector coupled monostable multivibrator is given by
a) T = 0.69RC b) T = 1.38RC c) T = RC d) T = 0.707RC

25. The frequency of oscillation of astable multivibrator with $R_1 = R_2 = 1k\Omega$, $C_1 = C_2 = 1\mu F$ is
a) (1/1.38)kHz b) 1.38kHz c) (1/38)Hz d) 13.8Hz

26. Advantages of emitter coupled astable over collector coupled circuit is
a) it is inherently self starting b) o/p is free of recovery transients
c) it has an isolated i/p d) all of these

27. Sine wave can be converted into square wave using
a) monostable b) schmitt trigger
c) clamping circuit d) astable multivibrator

28.Satandard pulse generator usually employs _____ multivibrator
a) astable b) monostable c) bistable d) none

29.Bistable multivibrator differ from astable multivibrator in the use of _____ between states instead of RC coupling .
a) triggering b) resistors c) capacitors d) none

30. Which of following is known as voltage to time converter.
a) monostable b) bisatble c) astable d) schmitt trigger

31. Which of the following is known as voltage to frequency converter
a) astable b) bisatble c) monostable d) schmitt trigger

32. Which of the following is used in frequency division
a) positive b) negative c) either positive (or) negative d) none

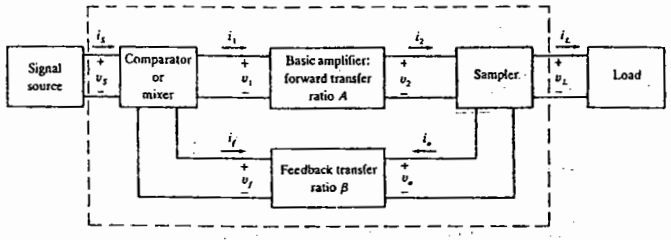
## KEY -- OBJECTIVE QUESTIONS

| | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| 1. d | 2. a | 3. a | 4. b | 5. c | 6. b | 7. a | 8. a | 9. b | 10. c | |
| 11. c | 12. b | 13. c | 14. a | 15. b | 16. d | 17. a | 18. a | 19. c | 20. c | 21. c |
| 22. b | 23. c | 24. a | 25. a | 26. d | 27. b | 28. b | 29. a | 30. a | 31. a | 32. a |

## Chapter: 6 FEEDBACK AMPLIFIERS AND OSCILLATORS

# Feedback amplifiers

A general feedback amplifier structure is shown below:



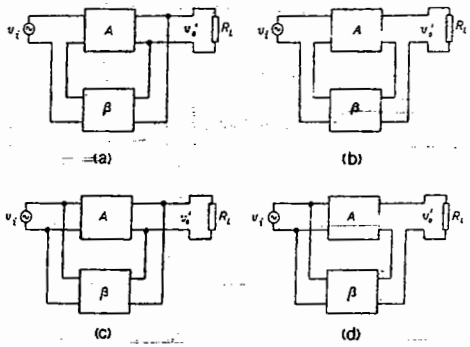

The input signal is applied to a mixer network, where it is combined with a feedback signal. The resultant signal from the mixer is applied to the basic amplifier. The amplifier output is sampled and applied to a feedback network. The output of feedback network is fed to a mixer. If the feedback signal is of opposite polarity to the input signal, negative feedback results. While negative feedback results in reduced overall gain, a number of improvements are obtained, among them being.

1. Stabilization of gain
2. Improved frequency response
3. Reduced noise
4. More linear operation

***FEED BACK CONNECTION TYPES →***

There are four basic ways of connecting the feedback signal. Both voltage and current can be fed back to the input either in series or parallel. Specifically there can be

1. Voltage – series feedback (fig-a)
2. Voltage – shunt feedback (fig-c)
3. Current – series feedback (fig-b)
4. Current – shunt feedback (fig-d)



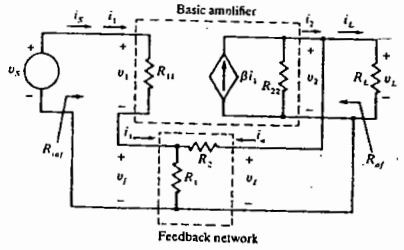

Here voltage refers to connecting the output voltage as input to the feedback network; current refers to tapping off some output current through the feedback network. Series refers to connecting the feedback signal in series with the input signal voltage; shunt refers to connecting the feedback signal in shunt with an input current source.

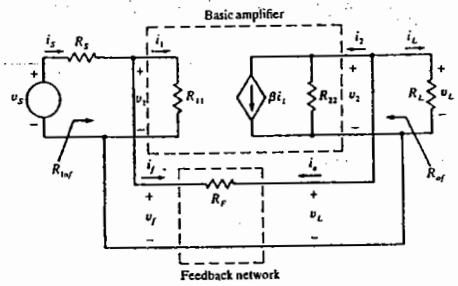
Series feedback connection tends to increase the input resistance while shunt feedback connection tends to decrease the input resistance. Voltage feedback tends to decrease the

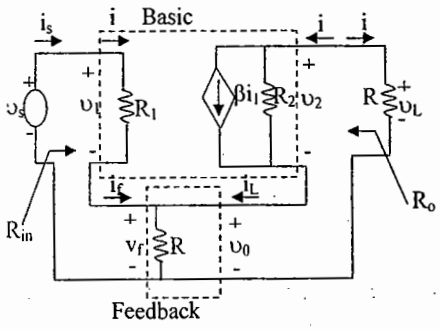


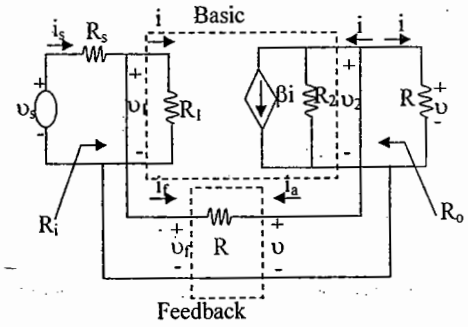
output impedance while current feedback tends to increase the output impedance. Typically, higher input and lower output impedances are desired for most cascade amplifiers. Both of these are provided using the voltage – series feedback connection.

The four feedback configurations with basic amplifier in its equivalent circuit form and feedback network with resistances are indicated below

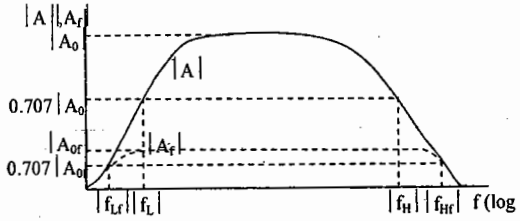



***Effect of Negative Feedback on Gain and Band width →***




The above figure shows that the amplifier with negative feedback has more bandwidth ($B_f$) than the amplifier without feedback (B).The feedback amplifier has a higher upper 3-dB frequency. In fact, the product of gain and frequency remains the same so that the gain band width product of the basic amplifier is the same value for the feed back amplifier.

***Gain Stability with Feedback →***

$$\left|\frac{dAf}{Af}\right| = \frac{1}{|1+\beta A|}\left|\frac{dA}{A}\right|$$

$$\left|\frac{dAf}{Af}\right| \cong \left|\frac{1}{\beta A}\right|\left|\frac{dA}{A}\right| \quad \text{for } \beta A >> 1$$

This shows that magnitude of the relative change in gain $\left|\frac{dA_f}{A_f}\right|$ is reduced by the factor $\beta A$ Compared to that without feedback $\left(\left|\frac{dA}{A}\right|\right)$

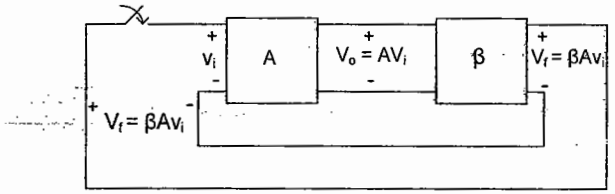
| Parameter | Voltage series | Current shunt | Voltage shunt | Current series |
|---|---|---|---|---|
| 1. Output signal | Voltage | Current | Voltage | Current |
| 2. Input Signal | Voltage | Current | Current | Voltage |
| 3. Basic amplifier | Voltage | Current | Transresistance | Transconductance |
| 4. A(With out feedback) | $A_V = V_0/V_i$ | $A_I = I_0/I_i$ | $R_m = V_0/I_i$ | $G_m = I_0/V_i$ |
| 5. $\beta$ | $V_f/V_0$ | $I_f/I_0$ | $I_f/V_0$ | $V_f/I_0$ |
| 6. $D=1+A\beta$ | $1+A_V\beta$ | $1+A_I\beta$ | $1+R_m\beta$ | $1+G_m\beta$ |
| 7. $A_f$ | Av/D | $A_I/D$ | $R_m/D$ | $G_m/D$ |
| 8. $R_{if}$ | Ri.D | $R_i/D$ | $R_i/D$ | Ri.D |
| 9. $R_{of}$ | Ro/D | Ro.D | Ro/D | RoD |
| 10. $f_{1f}$ | $f_1/D$ | $f_1/D$ | $f_1/D$ | $f_1/D$ |
| 11. $f_{2f}$ | $f_2.D$ | $f_2.D$ | $f_2.D$ | $f_2.D$ |
| 13. $BW_f$ | ≅. BW.D | ≅. BW.D | ≅. BW.D | ≅. BW.D |
| 14. $d_f$ (distortion) | =d/D | =d/D | =d/D | =d/D |
| 15. Noise | Decreases | Decreases | Decreases | Decreases |

***Oscillators:*** The use of positive feedback which results in a feedback amplifier having closed-loop gain $A_f$ greater than 1 and satisfying the phase conditions will result in operation as an oscillator circuit.To understand how a feedback circuit performs as an oscillator consider the feed back circuit below.

When the switch at the amplifier output is open, no oscillation occurs. Consider that we have a fictitious voltage at the amplifier input ($V_i$). This results in an output voltage $V_0 = AV_i$ after the amplifier stage and in a voltage $V_f = \beta(AV_i)$ after the feedback stage. Thus, we have a feedback voltage $V_f = \beta AV_i$, where $\beta A$ is referred to as the loop gain. If the circuits of the



base amplifier and feed back network provide $\beta A$ of a correct magnitude and phase, $V_f$ can be made equal to $\beta V_i$.




Then, when the switch is closed and fictitious voltage $V_i$ is removed, the circuit will continue operating since the feedback voltage is sufficient to drive the amplifier and feed back circuits resulting in a proper input voltage to sustain the loop operation. The output waveform will still exist after the switch is closed. The condition $\beta A = 1$ is met. This is known as the Barkhausen Criterion for oscillation.

In reality, no input signal is needed to start the oscillator going. Only the condition $\beta A = 1$ must be satisfied for self sustained oscillations to result. In practice $\beta A$ is made greater than 1, and the system is started oscillating by amplifying noise voltage which is always present.

Another way of seeing how the feed back circuit provides operation as an oscillator is obtained by noting the denominator in the basic feed back equation. $A_f = A / (1+ \beta A)$. When $\beta A = -1$ or magnitude 1 at a phase angle of 180°, the denominator becomes 0 and the gain with feedback, $A_f$, becomes infinite. Thus, an infinitesimal signal can provide a measurable output voltage, and the circuit acts as an oscillator even without an input signal.

***Phase- Shift Oscillator:***

Using classical network analysis, we find that

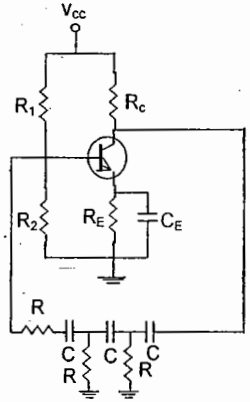
$$f = \frac{1}{2\pi RC\sqrt{6}}$$

$$\beta = \frac{1}{29}$$

and the phase shift is 180°

For the loop gain A to be greater than unity the gain of the amplifier stage must be greater than $1/\beta$ or 29:

$$A > 29$$




The frequency given above is that at which the total phase shift is 180°. If one measured the phase shift per RC section, each section would not provide the same phase shift. If it were desired to obtain exactly a 60° phase shift for each of three stages, then emitter-follower stages would be needed for each RC section to prevent each from being loaded from the following circuit.

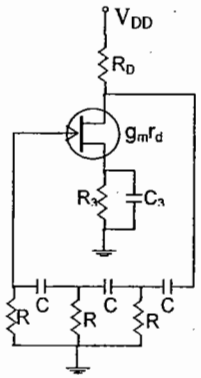
Analysis of the ac circuit provides the following equation for the resulting oscillator frequency:

$$f = \frac{1}{2\pi RC}\quad\frac{1}{\sqrt{6}+4(R_C/R)}$$

For the loop gain to be greater than unity, the requirement on the current gain of the transistor is found to be

$$h_{fe} > 23 + 29\frac{R}{R_c} + 4\frac{R_c}{R}$$

***FET phase shift Oscillator:***

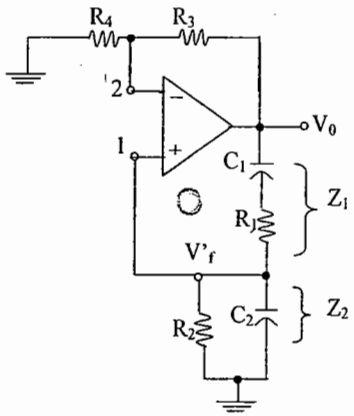



The amplifier stage is self biased with a capacitor bypassed source resistor $R_S$ and a drain bias resistor $R_D$. The FET device parameters of interest are $g_m$ and $r_d$.

$A = g_m R_L$ where $R_L = \dfrac{R_D r_d}{R_D + r_d}$

It is assumed that the input impedance of the FET amplifier stage is infinite.

***Wien Bridge Oscillator →***




The figure shows a basic version of a Wien bridge oscillator circuit. Resistors $R_1$, $R_2$ and capacitors $C_1$,$C_2$ form the frequency adjustment elements, while resistors $R_3$ and $R_4$ form part of the feedback path. Neglecting the loading effects of the op-amp input and output impedances, the analysis of the bridge circuit results in

$$\frac{R_3}{R_4} = \frac{R_1}{R_2} + \frac{C_2}{C_1}$$

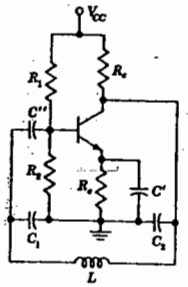
And $f_0 = \dfrac{1}{2\pi\sqrt{R_1 C_1 R_2 C_2}}$

If, in particular, the values are $R_1 = R_2 = R$ and $C_1 = C_2 = C$, the resulting oscillator frequency is

$$f_0 = \frac{1}{2\pi RC}$$

and $\dfrac{R_3}{R_4} = 2$

Thus a ratio of $R_3$ to $R_4$ greater than 2 will provide sufficient loop gain for the circuit to oscillate.




***Tuned Oscillator Circuit →***

Colpitts Oscillator:

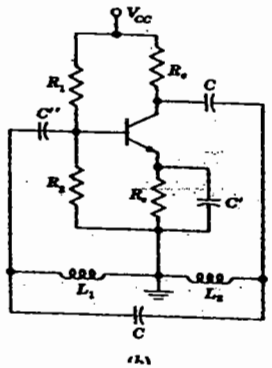
The oscillator frequency can be found to be

$$f_0 = \frac{1}{2\pi\sqrt{LC_{eq}}}$$

Where $C_{eq} = \dfrac{C_1 C_2}{C_1 + C_2}$



***Hartley Oscillator:***




The inductors $L_1$ and $L_2$ have a mutual coupling, M, which must be taken into account in determining the equivalent inductance for the resonant tank circuit. The circuit frequency of oscillation is then given approximately by

$$f_0 = \frac{1}{2\pi\sqrt{L_{eq} C}}$$

With $L_{eq} = L_1 + L_2 + 2M$

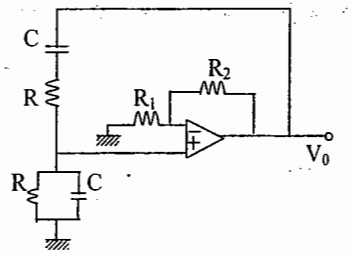
***Crystal Oscillator →*** A crystal oscillator is basically a tuned – circuit oscillator using a piezoelectric crystal as a resonant tank circuit. The crystal (usually quartz) has a greater stability in holding constant at whatever frequency the crystal is originally cut to operate. Crystal oscillators are used whenever great stability is required, for example, in communication transmitters and receivers.

# OBJECTIVES SET - A

1. In a common Emitter amplifier the unbypassed emitter resistance provides
   a) Voltage shunt feedback
   b) Current series feedback
   c) Negative voltage feedback
   d) Positive-current feedback

2. A Wien bridge oscillator is shown in the figure. Which of the following statements are true, if 'f' is the frequency of oscillation?

   a) For R =1K, C= $\frac{1}{2\pi}$ μF, f=1KHZ
   b) For R = 3K. C = $\frac{1}{18\pi}$ μF, f = 3KHz
   c) The gain of the op-amp stage should be less than two for proper operation.
   d) The gain of the op-amp stage should be three for proper operation.

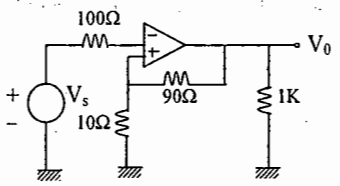



3. A practical R-C sinusoidal oscillator is built using a positive feedback amplifier with a closed loop gain slightly less than unity. FALSE/TRUE

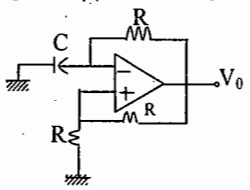
4. The voltage series feedback in a feedback amplifier leads to increase in band width, while the voltage gain becomes less sensitive
   a) decrease in overall gain, while the input resistance decreases
   b) increase in distortion, while the output resistance decreases
   c) decrease in input resistance, while the output resistance increases.

5. The feedback factor for the circuit shown is

   a) 9/100
   b) 9/10
   c) 1/9
   d) 1/10

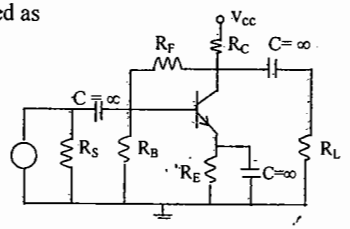



6. For the oscillator circuit shown in figure, the expression for the time period of oscillation can be given by (where $\tau = RC$)
   a) $\tau \ln 3$
   b) $2\tau \ln 3$
   c) $\tau \ln 2$
   d) $2\tau \ln 2$





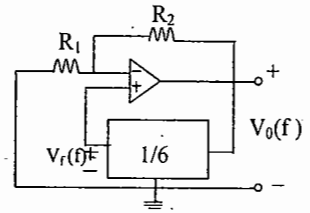

7. The feedback used in the circuit can be clarified as
   a) shunt-series feedback
   b) shunt-shunt feedback
   c) series-shunt feedback
   d) series-series feedback



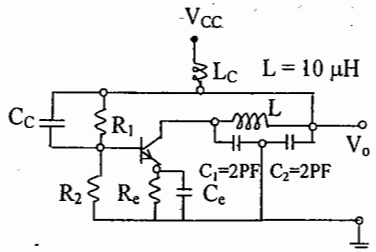

8. An amplifier without feedback has a voltage gain of 50, input resistance of 1KΩ and output resistance of 2.5KΩ. The input resistance of the current-shunt negative feedback amplifier using the above amplifier with a feedback factor of 0.2 is
   a) 1/11 kΩ b) 1/5kΩ c) 5kΩ d) 11kΩ

9. In a negative feedback amplifier using voltage-series feedback
   a) $R_i$ decreases and $R_0$ decreases
   b) $R_i$ decreases and $R_0$ increases
   c) $R_i$ increases and $R_0$ decreases
   d) $R_i$ increases and $R_0$ increases

10. The circuit in figure employs a positive feedback and is intended to generate sinusoidal oscillations. If at a frequency $f_0$, loop gain $= 1 \angle 0°$, then to sustain oscillations at this frequency
    a) $R_2 = 5R_1$
    b) $R_2 = 6R_1$
    c) $R_2 = R_1/6$
    d) $R_2 = R_1/5$




11. The oscillator circuit is
    (a) Hartley oscillator with $f_{osc} = 79.6$ MHz
    b) Colpitts oscillator with $f_{ox} = 79.6$ MHz
    c) Hartley oscillator with $f_{osc} = 159.2$ MHz
    d) Colpitts oscillator with $f_{osc} = 159.2$MHz




12. A higher-Q quartz crystal exhibits series resonance at the frequency $\omega_s$ and parallel resonance at the frequency $\omega_p$. Then
    a) $\omega_s$ in very close to, but less than $\omega_p$
    b) $\omega_s << \omega_p$
    c) $\omega_s$ in very close to, but greater than $\omega_p$
    d) $\omega_s >> \omega_p$

13. Introduction of feedback in an amplifier increases the input impedance from 1KΩ to 40KΩ. It is due to

a) positive feedback
b) shunt-current negative feed back
c) series-current negative feed back
d) shunt-voltage negative feed back

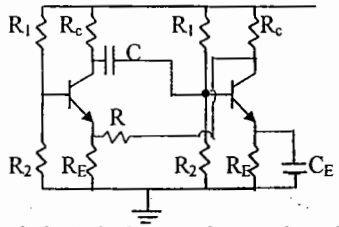
14. A radio frequency signal contains three frequencies:870 KHz, 875 KHz and 880 KHz. This signal needs to be amplified. The amplifier used should be

a) audio frequency amplifier
b) wide-band amplifier
c) tuned voltage amplifier
d) push-pull amplifier

15. An emitter follower circuit is widely used in electronic instruments because

a) its voltage gain is less than unity
b) its output impedance is high and input impedance is low
c) its output impedance is low and input impedance is high
d) its voltage gain is very high

16. In the circuit shown in fig.the feed back causes




a) An increase in both the input and output impedances.
b) An increase in the input impedance but a decrease in the output impedance.
c) An decrease in both the input and output impedances.
d) A decrease in the input impedance but an increase in the output impedance.

17. The voltage gains of an amplifier without feedback and with negative feed back respectively are 100 and 20.The percentage of negative feedback(β) would be

a) 40% b) 5% c) 20% d) 80%



18. If the Q of a single stage single- tuned amplifier is doubled, then its bandwidth
a) remains same b) becomes half c) becomes double
d) becomes four times

19. The negative feedback in an amplifier

(a) reduces the voltage gain
(b) increases the voltage gain
(c) does not affect the voltage gain
(d) can convert it into an oscillator if the amount of feedback is sufficient

20. Introduction of feedback in an amplifier increases the input impedance from 1 kΩ to 40 kΩ. It is due to

(a) positive feedback
(b) shunt-current negative feedback
(c) series-current negative feedback
(d) shunt-voltage negative feedback

21. One of the effects of negative feedback in amplifiers is to

(a) increase the noise
(b) increase the harmonic distortion
(c) decrease the bandwidth
(d) decrease the harmonic distortion

22. Positive feedback, in an amplifier circuit will ..... the gain of the amplifier.
(a) increase (b) decrease, (c) not alter

23. Gain stability in an amplifier can be improved by using

(a) positive feedback,
(b) negative feedback,
(c) both positive and negative feedback.

24. Effect of voltage negative feedback on the input impedance of an amplifier.

(a) increase (b) decrease (c) not altered

25. Effect of voltage negative feedback on the output impedance of an amplifier

(a) increase (b) decrease (c) not altered

26. Application of current negative feedback will

(a) increase the input impedance
(b) increase the output impedance
(c) increase both the input and output impedances

27. An emitter follower is an example of

(a) current negative feedback
(b) voltage negative feedback
(c) neither voltage feedback nor current negative feedback.

28. An emitter follower has a input impedance value.

(a) large (b) small (c) very small

29. An emitter follower has a output impedance value.

(a) small (b) large (c) very large

30. With negative feedback, the bandwidth of an amplifier can be

(a) increased (b) decreased (c) neither increased nor decreased

31. A emitter-follower amplifier can help to

(a) match a low-resistance source with a high-resistance load
(b) match a high-resistance source with a low-resistance load
(c) match equal values of source resistance and load resistance

32. In a multistage amplifier, application of negative feedback can

(a) produce stability in all cases (b) produce instability in some cases
(c) produce instability in all cases

33. With negative feedback, the gain-bandwidth product of an amplifier would be

(a) increased (b) decreased (c) neither increased nor decreased

34. The main advantage of applying negative feedback to an amplifier is to

(a) increase the amplifier gain (b) decrease the amplifier- gain
(c) make the amplifier oscillate (d) improve the amplifier stability

35. A negative feedback amplifier, with A=1000 and β=0.20, will have an overall gain of about
(a) 20 (b) 200 (c) 50 (d) 5 (e) -5

36. In a negative feedback voltage amplifier, with A = 1000 and β = 0.2 there is an unwanted hum voltage of 1V at its output before feedback is applied. With negative feedback, the hum voltage will be
(a) 1 V (b) 0.2 V (c) 5 mV (d) 1 mV.

37. In a negative feedback voltage amplifier, with A=1000 and β =0.2, the input resistance is 1 KΩ before voltage negative feedback is applied. After negative feedback, the input resistance will be
(a) 200 KΩ (b) 5 Ω (c) 1 MΩ (d) 5 KΩ

38. In a current amplifier, with A=1000 and β=0.20, the output resistance is 100 Ω before current negative feedback is applied. After negative feedback is applied, its output resistance will be
(a) 0.5 Ω (b) 20 KΩ (c) 500 Ω (d) 20

39. For generating a 1-kHz note, the most suitable circuit is
(a) Hartley oscillator (b) Colpitts oscillator
(c) tuned-collector oscillator (d) Wien bridge oscillator

40. To generate a 1-MHZ signal, the most suitable circuit is
(a) Wien bridge oscillator (b) phase-shift oscillator
(c) Colpitts oscillator (d) none of the above



41. We use a crystal oscillator because
(a) it gives high output voltage (b) it works at high efficiency
(c) the frequency of oscillations remains substantially constant
(d) it requires very low dc supply voltage

42. Oscillator is a
a) ac to dc converter b) dc to ac converter c) none

43. The condition which is required to get sustained oscillation is called
a) Barkhausen criteria b) $|AB| = 1$
c) The total phase shift introduced by both amplifier and feedback network must be equal to zero (or) multiples of $2\pi$ radians
d) all of the above

44. In transistor tuned oscillator, frequency of oscillations is determined by
a) RC network b) Tank circuit c) RC parallel circuit d) None

45. The minimum gain required by transistor, when it is used in RC phase shift oscillator is
a) 44.5 b) 29 c) 3 d) None

46. The minimum gain is 29, when ------- is used in RC phase shift oscillator
a) Transistor b) FET c) Tank circuit d) None

47. In RC phase shift oscillator, phase shift introduced by each RC network is
a) $45^0$ b) $90^0$ c) $60^0$ d) $180^0$

48. In Hartley oscillator, feedback network consists of ------
a) Two inductors b) One capacitor c) Both a & b d) None

49. In Colpitts oscillator, feedback network consists of -------
a) Two capacitors b) One inductor c) Both a & b d) None

50. The minimum gain required by the amplifier is -------, when it is used as a Wien-bridge oscillator
a) 3 b) $\sqrt{29}$ c) 44.5 d) None

51.-----is used as a feedback network in a Wien-bridge oscillator
a) Feedback amplifier b) Wien-Bridge c) RC network d) None

52.The phase shift introduced by Wien bridge is-----
a) $90^0$ b) $180^0$ c) $0^0$ d) zero

53. Limitation of LC & RC oscillators: their frequency of operation varies with
a) temperature b) LC network c) RC network d)None

54. Crystals are used to convert mechanical energy into electrical energy & vice versa. This phenomena is known as
a) Piezo conductive effect b) Piezo magnetic c) Piezo electric effect d) None

55. Piezo electric effect is used in the following crystals
a) Rochelle salt b) Quartz c) both a & b d) None

56. In transistor RC phase shift oscillator the type of feedback used is ----
a) voltage - shunt b) voltage - series c) current -shunt d) current - series

57.In FET RC phase shift oscillator the type of feedback used is------
a) voltage - shunt b) voltage - series c) current - shunt d) current - series

58. In LC tuned oscillator the frequency of oscillations
a) $f=\frac{1}{2\pi RC\sqrt{6+4K}}$ b) $f=\frac{1}{2\pi RC\sqrt{6}}$ c) $f=\frac{1}{2\pi\sqrt{LC}}$ d) None

59. In transistor RC phase shift oscillator the frequency of oscillations is
a) $f=\frac{1}{2\pi RC\sqrt{6+\frac{R_C}{R}}}$ b) $f=\frac{1}{2\pi RC\sqrt{6+4R_C}}$
c) $f=\frac{1}{2\pi RC\sqrt{6+4R}}$ d) None

60. In FET RC phase shift oscillator the frequency of oscillations is
a) $f=\frac{1}{2\pi RC}$ b) $f=\frac{1}{2\pi RC\sqrt{6}}$ c) $f=\frac{1}{12\pi RC}$ d) None

61. In Hartley oscillator, the frequency of oscillations is
a) $f=\frac{1}{2\pi\sqrt{LC}}$ b) $f=\frac{1}{2\pi\sqrt{L_1C_1}}$ c) $f=\frac{1}{2\pi\left(\sqrt{L_1+L_2}\right)C}$ d) None

62. In Colpitts oscillator circuit, frequency of oscillation is
a) $f=\frac{1}{2\pi\sqrt{L\left(\frac{c_1c_2}{c_1+c_2}\right)}}$ b) $f=\frac{1}{2\pi\sqrt{LC}}$ c) $f=\frac{1}{2\pi\sqrt{L_1C_1}}$ d) None

63. In Wien bridge oscillator, frequency of oscillations is
a) $f=\frac{1}{2\pi\sqrt{RC}}$ b) $f=\frac{1}{2\pi RC}$ c) $f=\frac{1}{2\pi R_1C_1}$ d) none

64. Frequencies that can be obtained with crystals are within the range
a) 25 kHz to 5 MHz b) 20 to 20 kHz c) 20 kHz to 10 MHz d) none

65. In tuned collector L = 50mH , C= 20PF is used.The frequency of operation is
a) $10^6$ MHz b) $10^6/2\pi$ Hz c) $2\pi/10^6$ Hz d) none

66. In FET RC phase oscillator, if the value of R is doubled, then frequency of operation is
a) f= $1/2\pi RC$ b) $f=\frac{1}{2\pi RC\sqrt{3}}$ c) $f=\frac{1}{2\pi RC\sqrt{6}}$ d) none

67. RC phase shift oscillator can have _____ RC stages in β network
a) 3 b) 4 c) 6 d) all of the above



68. In Wien bridge oscillator $R_1 = R_2 = 100$ kHz, $C1 = C_2 = 0.01$ μF. The frequency of oscillations is
a) 0.16 kHz b) 0.16 Hz c) 1 kHz d) none

69. Frequency of oscillations of RC phase shift oscillator is
a) impossible to vary b) difficult to vary c) always variable d) none

70. A crystal has L = 3.3H , $C_S$ = 0.042pF, R = 390 Ω,If the crystal operates at 430 kHz, the Q of the crystal is
a) 23 b) 230 c) 23000 d) none

71. RC phase shift oscillator can have
a) $f_0=\frac{\sqrt{6}}{2\pi RC}$ b) $f_0=\frac{1}{2\pi RC\sqrt{6}}$ c) both a & b d) none

72.The oscillation frequency of a transistor Colpitts oscillator is ($C_1 = C_2 = 0.1\mu F$, $L = 200\mu H$)
a) 0.16 MHz b) 0.16 Hz c) 0.16 kHz d) none

73. The operating frequency of a transistor Hartley oscillator, if $L_1 = 25mH, L_2 = 25mH$, C = 20pF, is
a) 0.16Hz b) 0.06Hz c) 0.16mHz d) none

74.In Wien bridge oscillator gain & frequency are
a) $|A|\geq 3, f_0=\frac{1}{2\pi RC}$ b) $|A|\geq 2, f_0=\frac{1}{2\pi RC}$
c) $|A|\geq 29, f_0=\frac{1}{2\pi\sqrt{6}RC}$ d) $|A|\geq 29, f_0=\frac{1}{2\pi RC}$

75. An electronic oscillator is
a) an amplifier b) an amplifier with negative F/B
c) converter of ac to dc d) converter of dc to ac

76. In BJT RC phase shift oscillator, $f_0$ is
a) $f_0=\frac{1}{2\pi\sqrt{6+4kRC}}$ b) $f_0=\frac{\sqrt{6+4k}}{2\pi R}$ c)both a and b d) none

77. In crystal oscillator, frequency determining parameters are
a) thickness of crystal b) angle of cut
c) physical size of crystal d) all of the above

78. To generate 1MHz frequency the most suitable oscillationr is
a) phase shift b) Wien bridge c) Colpitts d) none

79. For generating 1kHz frequency the most suitable oscillator is
a) tuned oscillator b) Hartely c) Colpitts d) Wien bridge

80. The Q of a crystal is of the order of
a) 100 b) 1000 c) 50 d) more than 10000

81. Crystal oscillator is commonly used in
a) laboratories b) radio receivers c) radio transmitters d) none

82. _____ oscillator is a fixed frequency oscillator
a) Wien bridge b) Crystal c) Hartley d) Colpitts

83. To change the frequency of crystal oscillator, we should change
a) gain of the amplifier b) DC power supply c) crystal thickness d) none

84. In a particular oscillator circuit if the value of β is 1/ 100, the min. gain required by the amplifier to get sustained oscillations is
a) 10 b) 1000 c) 200 d) 100

85. In order to produce frequencies in the microwave region one should use _____ oscillator.
a) Wien bridge b) crystal c) both (a) &(b) d) none

86. Frequency stability of RC oscillator is _____ than LC oscillator.
a) greater b) lower c) same as d) none

87. In tuned collector oscillator if L value is multiplied by four, the frequency of oscillation is
a) is halved b) doubles c) is reduced by four times d) remains constant

88. In BJT RC –phase shift oscillator, condition for sustained oscillations is
a) $h_{fe} \geq 4k + 23 + \frac{49}{k}$ b) $h_{fe} \geq \frac{L_b}{L_a}$ c) $h_e \geq \frac{L_b}{L_a} + \frac{h_{ie}}{RC}\frac{L_a}{L_b}$ d) none

89. In RC –oscillators, using gang capacitors, $\frac{f_0 \max}{f_0 \min}$ is
a) 10 b) 3.3 c) $\frac{1}{10}$ d) $\frac{1}{3.3}$

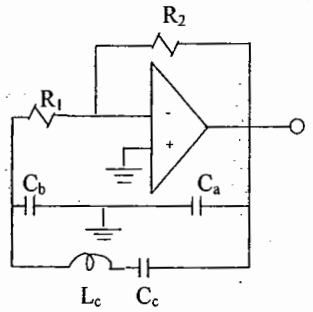
90. In LC oscillators using gang capacitors , $\frac{f_0 \max}{f_0 \min}$ is
a) 10 b) 3.3 c) $\frac{1}{10}$ d) $\frac{1}{3.3}$



91. In Hartley oscillator with inverting op-amp, condition for sustained oscillations is
a) $\left|\frac{R_2}{R_1}\right| \geq \frac{L_b}{L_a}$ b) $\left|\frac{R_2}{R_1}\right| \geq \frac{L_b}{L_a} + \frac{h_{ie}}{R_C}$ c) $\left|1 + \frac{R_2}{R_1}\right| \geq \frac{L_b}{L_a}$ d) none

92. In oscillators with $|A\beta| < 1$, we get
a) square wave b) sinusoidal c) both square and sinusoidal d) triangular

93. For Clapp oscillator circuit shown below , the expression for $f_0$ is
a) $f_0 = \frac{1}{2\pi\sqrt{L_C R_C}}$ b) $f_0 = \frac{1}{2\pi L_C R_C}$ c) $f_0 = \frac{1}{2\pi\sqrt{6}\sqrt{L_C R_C}}$ d) none




*KEY*

| | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1. b | 2. a,b,d | 3. false | 4. a | 5. d | 6. b | 7. b | 8. a | 9. c | 10. a | 11.b | |
| 12.a | 13.c | 14.c | 15.c | 16.b | 17.a | 18.b | 19.a | 20.c | 21.d | 22.a | 23.b |
| 24.a | 25.b | 26.b | 27.b | 28.a | 29.a | 30.a | 31.b | 32.a | 33.c | 34.d | 35.c |
| 36.c | 37.a | 38.a | 39.d | 40.c | 41. c | 42.b | 43.d | 44.b | 45.b | 46.b | 47.- |
| 48.c | 49.c | 50.a | 51. b | 52.c | 53.a | 54.c | 55.c | 56.a | 57.b | 58.c | 59.a |
| 60.b | 61.c | 62.a | 63.b | 64.a | 65.b | 66.c | 67.a | 68.a | 69.b | 70.c | 71.c |
| 72.a | 73.c | 74.a | 75. d | 76.c | 77.d | 78.c | 79.b | 80.b | 81.c | 82.b | 83.d |
| 84.d | 85.b | 86.b | 87.a | 88.a | 89.a | 90.b | 91.a | 92.a | 93. a | | |

## SET - B

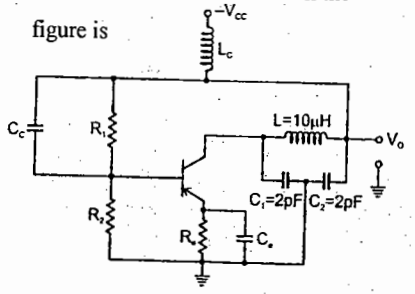
01. Negative feedback in an amplifier

(A) reduces gain
(B) increases frequency and phase distortions
(C) reduces bandwidth
(D) increases noise

02. An amplifier has an open – loop gain of 100, an input impedance of 1 kQ, and an output impedance of 100 Ω. A feedback network with a feedback factor of 0.99 is connected to the amplifier in a voltage series feedback mode. The new input and output impedances, respectively, are

(A) 10 Ω and 1 Ω
(B) 10 Ω and 10 Ω
(C) 100 kΩ and 1 Ω
(D) 100 kΩ and 1 kΩ

03. The oscillator circuit shown in the figure is




(A) Hartley oscillator with $f_{oscillation}$ = 79.6 MHz
(B) Colpitts oscillator with $f_{oscillation}$ = 50.3 MHz
(C) Hartley oscillator with $f_{oscillation}$ = 159.2 MHz
(D) Colpitts oscillator with $f_{oscillation}$ = 159.2 MHz

04. In a negative feedback amplifier using voltage-series (ie. voltage - sampling, series mixing) feedback.

(A) $R_i$ decreases and $R_o$ decreases
(B) $R_i$ decreases and $R_o$ increases
(C) $R_i$ increases and $R_o$ decreases
(D) Ri increases and $R_o$ increases

($R_i$ and $R_o$ denote the input and output resistances respectively)

05. An amplifier without feedback has a voltage gain of 50, input resistance of 1 K Ω and output resistance of 2.5 KΩ The input resistance of the current – shunt negative feedback amplifier using the above amplifier with a feedback factor of 0.2 is

(A) 1/11 K Ω (B) 1/5 KΩ
(C) 5 KΩ (D) 11 KΩ

06. Voltage series feedback (also called series – shunt feedback)results in

(A) increase in both input and output impedances
(B) decrease in both input and output impedances
(C) increase in input impedance and decrease in output impedance
(D) decrease in input impedance and increase in output impedance

07. The effect of current shunt feedback in an amplifier is to

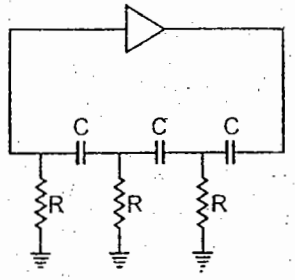
(A) increase the input resistance and decrease the output resistance
(B) increase both input and output resistances
(C) decrease both input and output resistances
(D) decrease the input resistance and increase the output resistance



08. In a transconductance amplifier, it is desirable to have.

(A) a large input resistance and a large output resistance
(B) a large input resistance and a small output resistance
(C) a small input resistance and a large output resistance
(D) a small input resistance and a small output resistance

09. The oscillator circuit shown in the figure has an ideal inverting amplifier. Its frequency of oscillations (in Hz) is




(A) $\frac{1}{(2\pi\sqrt{6}RC)}$
(B) $\frac{1}{(2\pi RC)}$
(C) $\frac{1}{(\sqrt{6}RC)}$
(D) $\frac{1}{\sqrt{6}\,(2\pi RC)}$

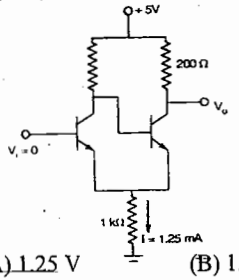
10. The input impedance ($Z_i$) and the output impedance ($Z_0$) of an ideal transconductance (voltage controlled current source) amplifier are

(A) $Z_i = 0, Z_o = 0$ (B) $Z_i = 0, Z_o = \infty$
(C) $Z_i = \infty, Z_o = 0$ (D) $Z_i = \infty, Z_o = \infty$

11. In a Common emitter amplifier, the unbypassed emitter resistance provides

(A) Voltage – shunt feedback
(B) Current – series feedback
(C) Negative – voltage feedback
(D) Positive – current feedback

12. In the Schmitt trigger circuit shown if $V_{CE(sat)}$ = 0.1 V, the output logic low level ($V_{OL}$) is




(A) 1.25 V (B) 1.35 V
(C) 2.50 V (D) 5.00 V

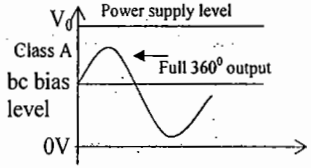
**KEY:** (1) A (2) C (3) B (4) C (5) A (6) C (7) D (8) A
(9) D (10) D (11) B (12) B

## Chapter: 7 Power Amplifiers

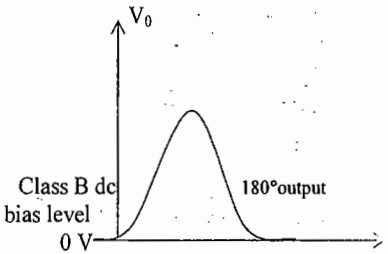
An amplifier receives a signal from the input source or some pick up transducer and provides a larger version of the signal to some output device or to another amplifier stage. Since signal voltage and current are small in a small signal amplifier, the amount of power handling capacity and power efficiency are of little concern. Large – signal or power amplifiers, on the other hand, primarily provide sufficient power to an output load to drive a speaker or other power device. Thus the power amplifier circuits are used to handle large voltage signals at moderate to high current levels and their main features include power efficiency, the maximum amount of power that the circuit is capable of handling and the impedance matching to the output device.

One method used to categorise amplifiers is by class of operation. Basically, amplifier classes represent the duration the output signal varies over one cycle of operation for a full duration of input signal.

***Class A*** : The output signal varies for a full 360° of the cycle. This requires the Q –point to be biased at a level so that at least half the signal swing of the output may vary up and swing down without going to a high enough voltage to be limited by the supply voltage level, or too low to approach the lower supply level.




***Class B*** : A class B circuit provides an output signal varying over one- half the input signal cycle, or for 180°. Here the dc bias is at cut off (zero current) So, the output is not a faithful reproduction of the input as only one half cycle is present. Two class B operations, one to provide output on the positive-output half cycle and another output to provide operation on the negative – output half cycle are necessary. This type of connection is referred to as push – pull operation.




***Class AB*** : An amplifier may be biased at a dc level above the zero base current level of class B and above one – half the supply voltage level of class. This bias condition is class AB. For class AB operation the output signal swing occurs between 180° and 360° and is neither class A nor class B operation.

***Class C*** : The output of a class C amplifier is biased for operation at less than 180° of the cycle and will operate only with a tuned (resonant) circuit which provides a full cycle of operation for the tuned or resonant frequency.

***Class D*** : This operating class is a form of amplifier operation using pulse signals which are on for a short interval and off for a longer interval. The major advantage of class D operation is that the amplifier is on only for short intervals and the overall efficiency can practically be very high.



*Amplifier Efficiency*: $\eta$

The power efficiency of an amplifier, defined as the ratio of power output to power input, improves (gets higher) going from class A to class D.

$$\%\eta = \frac{P_0(ac)}{P_i(dc)} \times 100\%$$

The larger the input signal, the larger the output swing up to the maximum set by the circuit. The ac power output delivered to the load($R_C$) can be expressed in a number of ways.

$P_0(ac) = V_{CE}(rms)\, I_C(rms) = I_C^2(rms)\, R_C = V_C^2\,(rms) / R_C$

Where $V_{CE}\,(rms) = V_{CE}\,(peak) / \sqrt{2}$

Using peak – to – peak signals : The ac power delivered to the load may be expressed using

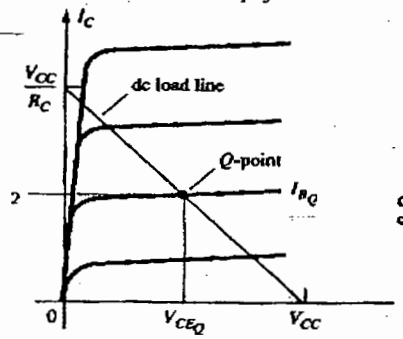
$$P_0(ac) = \frac{V_{CE}(p-p)\, I_C(p-p)}{8} = \frac{I_C^2(p-p)\, R_C}{8} = \frac{V_{CE}^2\,(p-p)}{8R_C}$$

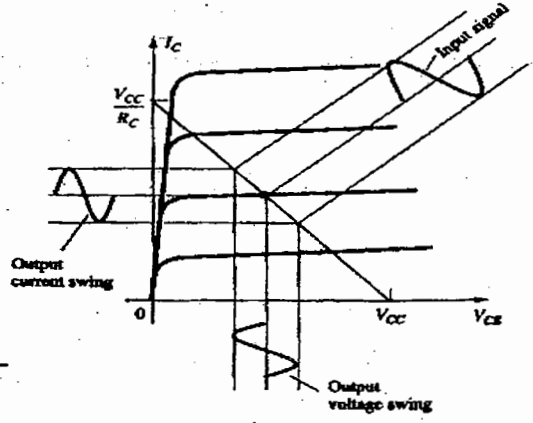
The power efficiency of an amplifier represents the amount of ac power delivered from the dc source.

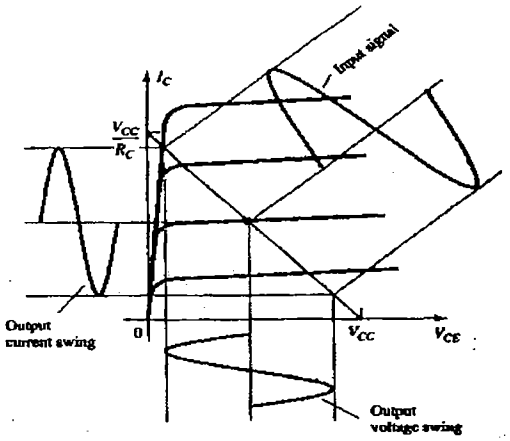
The maximum efficiency of a class A circuit, occurring for the largest output voltage and current swings, is only 25% with a direct or series fed load connection, and 50% with a transformer connection to the load. Class B operation, with no dc bias power for no input signal, can be shown to provide a maximum efficiency that reaches 78.5%.

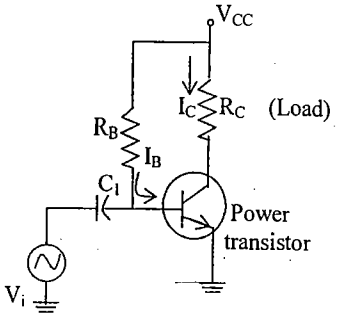
Class D operation can achieve power efficiency over 90% and provides the most efficient operation of all the operating classes. Since class AB falls between class A and class B in bias, it also falls between their efficiency ratings – between 25% (or 50%) and 78.5%.

*Series fed Class – A amplifier:*






$$P_i(dc) = V_{CC}\, I_C$$

Even with an ac signal applied, the average current drawn from the supply remains the same. The output voltage and current varying around the bias point provide ac power to the load. This ac power is delivered to the load, $R_C$, in the circuit. The ac signal, $V_i$, causes the base current to vary around the dc bias.

$V_{CE}(p-p) = V_{CC}$.
$I_C(p-p) = V_{CC} / R_C$.

Using the maximum voltage swing.

$$\text{Maximum } P_0(ac) = \frac{V_{CC}(V_{CC}/R_C)}{8}$$

$$= \frac{V_{CC}^2}{8\,R_C}$$

The maximum power output can be calculated using the dc bias current set to half the maximum value.

$$\text{Maximum } P_i(dc) = V_{CC}(\text{maximum } I_C)$$

$$= V_{CC} \cdot \frac{V_{CC}/R_C}{2} = \frac{V_{CC}^2}{2R_C}$$

Maximum % $\eta$ = 25%

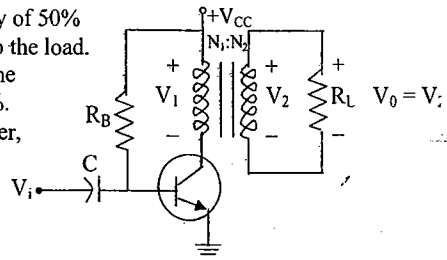
This maximum efficiency of a class A series fed amplifier is seen to be 25%. Since this efficiency will occur only for ideal conditions of both voltage swing and current swing, most series fed circuits will provide efficiencies of much less than 25%.



## Transformer Coupled Amplifier

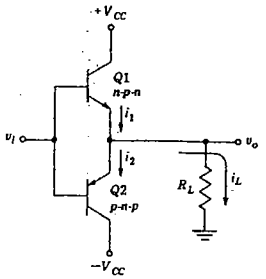
A class A amplifier having maximum efficiency of 50% uses a transformer to couple the output signal to the load. For a class A transformer – coupled amplifier the maximum theoretical efficiency goes up to 50%. Based on the signals obtained using the amplifier, the efficiency can be expressed as

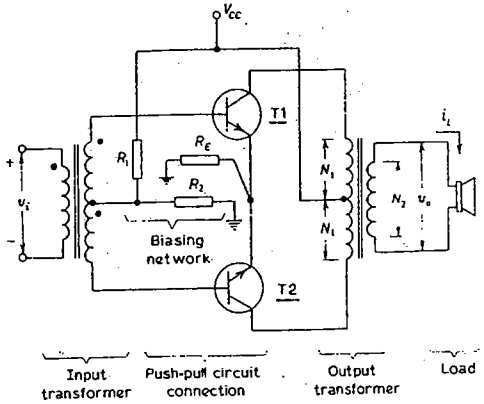
$$\%\eta = 50\% \left(\frac{V_{CEmax} - V_{CEmin}}{V_{CEmax} + V_{CEmin}}\right)^2$$




The larger the value of $V_{CEmax}$ and the smaller the value of $V_{CEmin}$, the closer the efficiency approaches the theoretical limit of 50%.

***Push pull amplifier***:




For class B operation the maximum output power is delivered to the load when $V_{L(p)} = V_{CC}$.

$$\text{Maximum } P_0(ac) = \frac{V_{CC}^2}{2R_L'}$$

The corresponding peak ac current $I_{(p)}$ is then

$$I_{(p)} = \frac{V_{CC}}{R_L'}$$

So that the maximum value of average current from the supply is maximum

$$I_{dc} = \frac{2\,I_P}{\pi} = \frac{2V_{CC}}{\pi R_L'}$$

$$\therefore \text{Maximum } P_i(dc) = V_C(\text{maximum } I_{dc}) = V_{CC}\left(\frac{2V_{CC}}{\pi R_L'}\right) = \frac{2V_{CC}^2}{\pi R_L'}$$

$$\text{Maximum } \%\eta = \frac{P_0(ac)}{P_i(dc)} \times 100\% = \frac{\pi}{4} \times 100\% = 78.54\%$$

For $V_{min} \neq 0$, the circuit efficiency is less than 78.5%.For class B operation the maximum power dissipated by the output transitions does not occur at the maximum power input or

output condition. The maximum power dissipated by the two output transistors occurs when the output voltage across the load is

$$V_{L(P)} = 0.636V_{CC}(= \frac{2}{\pi} V_{CC})$$

For a maximum transistor power dissipation of

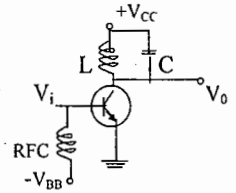
$$P_C(max) = \frac{2V_{CC}^2}{\pi^2 R_L'} = \frac{4}{\pi^2} P_0(max) \approx 0.4\, P_0(max)$$

For example, if it is desired to deliver 10W form a class B push – pull amplifier, $P_C(max) = 4W$. Hence transistors are to be selected with collector dissipation rating of 2W each.

*Class C:*

Class C amplifiers, while not used as audio amplifiers, do find use in tuned amplifiers.

The tuned circuit (L and C tank circuit) in the output of class C amplifier will provide a full cycle of output signal for the fundamental or resonant frequency of that tuned circuit (L and C tank circuit) of the output. This type of operation is therefore limited to use at one fixed frequency.




***Amplifier Distortion*** : A pure sinusoidal signal has a single frequency at which the voltage varies positive and negative by equal amounts. Any signal varying over less than the full 360° cycle is considered to leave distortion. When distortion occurs the output will not be an exact duplicate of the input signal. Distortion can occur because the device characteristics are not linear, in which case non linear or amplitude distortion occurs. This occurs with all classes of amplifier operation. Distortion can also occur because the circuit elements and devices respond to the input signal differently at various frequencies, this being frequency distortion.

A signal is considered to have harmonic distortion when there are harmonic frequency components. If the fundamental frequency has an amplitude, $A_1$, and the $n^{th}$ frequency component has an amplitude, $A_n$, a harmonic distortion can be defined as % $n^{th}$ harmonic distortion = $\% D_n = |A_n| / |A_1| \times 100\%$

The fundamental component is typically larger than any harmonic component,

When an output signal has a number of individual harmonic distortion components, the signal can be seen to have a total harmonic distortion based (THD)

$$\% THD = D = \sqrt{D_2^2 + D_3^2 + D_4^2 + \ldots\ldots\ldots} \times 100\%$$

For a signal occurring in class AB or class B, the distortion may be mainly due to even harmonics, of which the second harmonic component is the largest.

When distortion is present, the output power delivered to the load resistor $R_C$ due to the fundamental component of the distorted signal is $P_1 = I_1^2 R_C / 2$

The total power due to all the harmonic components of the distorted signal can then be

$$P = (I_1^2 + I_2^2 + I_3^2 + \ldots\ldots\ldots)\frac{R_C}{2}$$

The total power can also be expressed in terms of THD,

$$P = (1+D_2^2 + D_3^2 + \ldots\ldots\ldots)I_1^2 \frac{R_C}{2} = (1+D^2) P_1$$



## OBJECTIVES SET - A

1. A class A transformer coupled, transistor power amplifier is required to deliver a power output of 10 watts. The maximum power rating of the transistor should not be less than.

   a) 3W b) 10W c) 20W d) 40W

2. A power amplifier delivers 50W output at 50% efficiency. The ambient temperature is 25°C. If the maximum allowable junction temperature is 150°C, then the maximum thermal resistance $\phi_{jc}$ that can be tolerated is .....

3. Crossover distortion behaviour is characteristic of
   a) Class A output stage b) Class B output stage
   c) Class AB output stage d) Common – base output stage

4. The output power of a power amplifier is several times less than its input power: This is possible because
   (a) the power amplifier introduces negative resistance
   (b) the power amplifier converts a part of the input dc power into ac output power.
   (c) positive feedback exists in the circuit
   (d) step-up transformer is used in the circuit

5. The main function of the transformer used in the output of a power amplifier is
   (a) to step-up the voltage
   (b) to increase the voltage gain
   (c) to match the load impedance with dynamic output resistance of the transistor
   (d) to safeguard the transistor against overheating

6. Heat sinks are used in power amplifier circuits
   (a) to increase the output power
   (b) to reduce the heat losses in the transistor
   (c) to increase the voltage gain of the power amplifier
   (d) to increase the collector dissipation rating of the transistor

7. Match each of the member of column A with appropriate member of column B

| Column A | Column B |
|---|---|
| 1. Maximum efficiency of a class-B amplifier is | (a) 50 % |
| 2. Maximum efficiency of a class-A amplifier is | (b)78.5% |
| 3. Maximum efficiency of a class-C amplifier is | (c) 100% |

8. In a Class C transistor power amplifier, the base bias is
   (a) less than that corresponding to the collector current cut-off value,
   (b) equal to that corresponding to the collector current cut-off value,
   (c) more than that corresponding to the collector current cut-off value.

9. As compared to a Class B power amplifier, a Class C power amplifier gives..... of the current signal waveform.

   (a) less distortion (b) the same distortion (C) more distortion

10. In the case of a Class C power amplifier, the load must be
(a) a pure resistance (b) a parallel tuned circuit (c) a series tuned circuit.

11. The output tuned circuit, in a Class C power amplifier, must have
(a) a large Q value (b) a small Q value (c) a medium Q value.

12. In a Class A power amplifier, the angle of flow, of the device output current, is
(a) 90° (b) 180° (c) 360°

13. Class A power amplifier systems are
(a) linear (b) somewhat non-linear (c) non-linear.

14. Class B power amplifier systems are
(a) less efficient than Class A power amplifier systems
(b) more efficient than Class C power amplifier systems
(c) more efficient than Class A power amplifier systems but less efficient than Class C power amplifier systems.

15. Under non-signal conditions, a Class A power amplifier device as compared to a Class B power amplifier device dissipates
(a) less energy (b) more energy (c) same energy

16. A Class A power amplifier is used for amplifying
(a) wide-band audio frequency signals, (b) narrow-band high frequency signals,
(c) wide-band high frequency signals.

17. As compared to parallel operation, push-pull operation, of devices, gives rise to
(a) more distortion and less output, (b) less distortion and more output,
(c) less distortion and less output.

18. As compared to single-ended operation, push-pull operation of devices in amplifiers, causes ------ of the signal waveform.
(a) more distortion, (b) less distortion, (c) same distortion

19. Push-pull operation, of devices in amplifiers, helps to minimize (in the output signal waveform)
(a) odd harmonic components (b) even harmonic components
(c) neither odd harmonic nor even harmonic components.

20. The device rating, in the case of a Class A power amplifier, should correspond to
(a) only the non-signal condition (b) only the signal condition
(c) the non-signal as well as the signal condition.

21. A Class B power amplifier is termed as a linear system, if the load is
(a) a parallel-tuned circuit (b)a resistance (c) a transformer.

22. As compared to the impedance of the signal source, the input impedance of a voltage amplifier should be
(a) small (b) large (c) equal (d) infinite



23. A radio-frequency signal contains following three frequencies: 800kHz,875 kHz and 880 kHz. This signal needs to be amplified. The amplifier used should be
(a) audio-frequency amplifier (b) wide-band amplifier
(c) tuned voltage amplifier (d) push-pull amplifier

24. An amplifier of pass-band 450 kHz to 460 kHz will be named as
(a) wide-band amplifier (b) audio-frequency amplifier
(c) tuned voltage amplifier (d) video amplifier

25. A narrow-band amplifier is one that has a pass-band
(a) Limited to 2000 Hz only
(b) Limited to audio-frequency range only
(c) Approximately 10 % of its central frequency
(d) Somewhere in the region near the cut-off region of the active device used

26. Tuned voltage amplifiers are not used
(a) in public-address systems (b) in radio receivers
(c) where a band of frequencies is to be selected and amplified
(d) in television receivers

27. In a series resonant circuit, the impedance at resonance is
(a) minimum, and is equal to the resistance of the coil
(b) maximum and is equal to Q x R where Q is the quality factor of the coil and R is its resistance
(c) equal to 2R. where R is the coil resistance
(d) equal to R/2, where R is the coil resistance

28. For a series or parallel LC circuit, resonance occurs when
(a) $X_L$ is ten times $X_C$ (c) $X_L$ is equal to $X_C$
(b) $X_L$ is Q times $X_C$ (d) $X_C$ is 10 times $X_L$

29. An ac circuit resonates at 1000 kHz. It has a quality factor 50. The bandwidth (BW) and half-power points are
(a) BW = 10 kHz; $f_1$ = 1000 kHz; $f_2$ = 1010 kHz
(b) BW = 20 kHz; $f_1$ = 1000 kHz; $f_2$= 1020 kHz
(c) BW = 20 kHz; $f_1$= 990 kHz; $f_2$ = 1010 kHz
(d) BW = 10 kHz; $f_1$= 995 kHz; $f_2$= 1005 kHz

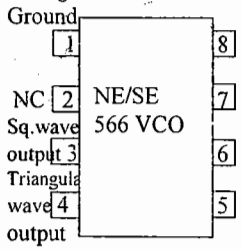
***KEY***

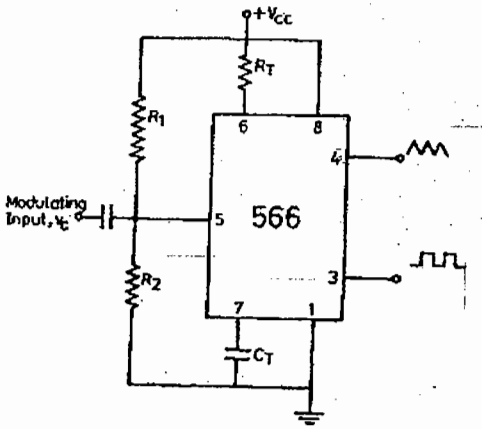
1. c 2. 5 ° C/W 3. b 4. b 5. c 6. d 7. 1-b, 2 – a, 3 – c 8. a 9. a 10. b

11. a 12. c 13. c 14. c 15. b 16. a 17. b 18. b 19. b 20. a 21. b

22. b 23. c 24. c 25. c 26. a 27. a 28. c 29. c

*Voltage Controlled Oscillator (VCO)→*




A common type of VCO available in IC form is signetics NE/SE 566. The pin configuration and basic block diagram of 566 VCO is shown above.

A timing capacitor $C_T$ is linearly charged or discharged by a constant current source/sink. The amount of current can be controlled by changing the voltage $V_C$ applied at the modulating input pin 5 or by changing the timing resistor $R_T$ external to IC chip. The voltage at pin 6 is held at the same voltage as pin 5.

The voltage across the capacitor $C_T$ is applied to the inverting input terminal of Schmitt trigger $A_2$ via buffer amplifier $A_1$. The output voltage swing of the Schmitt trigger is designed to $V_{CC}$ and 0.5 $V_{CC}$. When the voltage on the capacitor $C_T$ exceeds $0.5V_{CC}$ during charging, the output of the Schmitt trigger goes Low ($0.5V_{CC}$). The capacitor now discharges and when it is at $0.25V_{CC}$, the output of Schmitt trigger goes HIGH ($V_{CC}$). Since the source and sink currents are equal, capacitor charges and discharges for the same amount of time. This gives a triangular voltage waveform across $C_T$ which is also available at pin 4. The square wave output of the Schmitt trigger is inverted by inverter $A_3$ and is available at pin 3.

The frequency of oscillator $f_0$ is ,

$$f_0 = \frac{1}{T} = \frac{i}{0.5V_{CC}C_T} \quad \text{Where } i = \frac{V_{CC} - V_C}{R_T}$$

Where $V_C$ is the voltage at pin 5,

$$\therefore f_0 = \frac{2(V_{CC} - V_C)}{C_T R_T V_{CC}}$$

The output frequency of the VCO can be changed either by (i) $R_T$, (ii) $C_T$ or (iii) the voltage $V_C$ at the modulating input terminal pin 5.

A parameter of importance for VCO is voltage to frequency conversion factor $K_V$ and is defined as

$$K_V = \frac{\Delta f_0}{\Delta V_C}$$



Here $\Delta V_C$ is the modulation voltage required to produce the frequency shift $\Delta f_0$ for a VCO

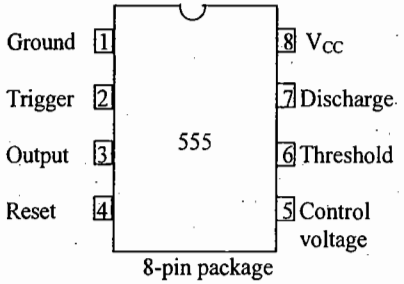
$$\Delta f_0 = f_1 - f_0$$

$$= \frac{2(V_{CC} - V_C + \Delta V_C)}{C_T R_T V_{CC}} - \frac{2(V_{CC} - V_C)}{C_T R_T V_{CC}}$$

$$= \frac{2\Delta V_C}{C_T R_T V_{CC}}$$

$$\Delta V_C = \frac{\Delta f_0 C_T R_T V_{CC}}{2}$$

**555 Timer→**




8-pin package

The three 5KΩ internal resistors act as voltage divider, providing bias voltage of 2/3 $V_{CC}$ to the upper comparator and 1/3 $V_{CC}$ to the lower comparator, where $V_{CC}$ is the supply voltage. Since these two voltages fix the necessary comparator threshold voltage, they also aid in determining the time interval. It is possible to vary time electronically too, by applying a modulation voltage to the control voltage input terminal (pin5). A negative going trigger pulse is applied to pin 2 and should have its dc level greater than the threshold level of the lower comparator ( i.e $V_{CC}$ /3). The reset input (pin 4) provides a mechanism to reset the FF in a manner which over rides the effect of any instruction coming to FF from lower comparator. The transistor $Q_2$ serves as a buffer to isolate the reset input from the FF and transistor $Q_1$. The transistor $Q_2$ is driven by an internal reference voltage $V_{ref}$ obtained from supply voltage $V_{CC}$.

**Monostable Operation →**

Voltage across the capacitor is given by

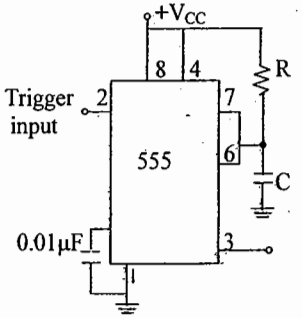
$$V_C = V_{CC}(1 - e^{-t/RC})$$

At t=T, $V_C = 2/3\ V_{CC}$

Therefore, $2/3\ V_{CC} = V_{CC}(1 - e^{-T/RC})$

Or $T = RC \ln(1/3)$

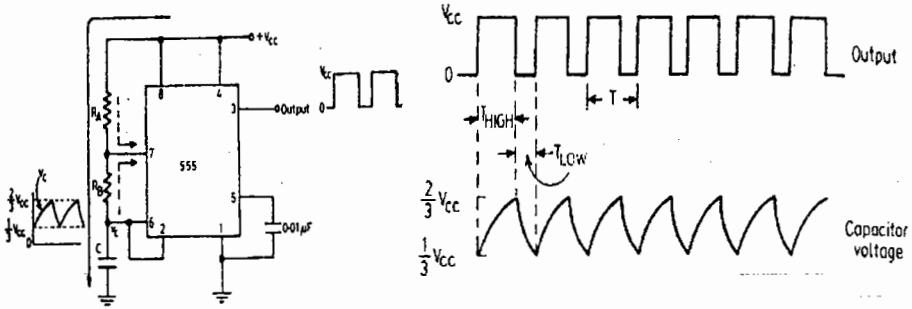
Or $T = 1.1\ RC$ seconds.




Missing pulse detector, Linear Ramp Generator, Frequency divider, pulse width Modulation are the applications of Monostable Operation of 555 timer.

output

**Astable Operation→**




Capacitor voltage for a low pass RC circuit subjected to a step input of $V_{CC}$ volts is given by

$$V_C = V_{CC}(1 - e^{-t/RC})$$

The time $t_1$ taken by the circuit to charge from 0 to 2/3 $V_{CC}$

$$2/3\ V_{CC} = V_{CC}(1 - e^{-t1/RC})$$

$$\text{or } t_1 = 1.09\ RC$$

and time $t_2$ to charge from 0 to 1/3 $V_{CC}$ is,

$$1/3\ V_{CC} = V_{CC}(1 - e^{-t2/RC})$$

$$\text{or } t_2 = 0.405\ RC$$

so the time to charge from 1/3 $V_{CC}$ to 2/3 $V_{CC}$ is

$$t_{High} = t_1 - t_2 = 0.69RC = 0.69\ (R_A + R_B)C.$$

The output is low while the capacitor discharges from 2/3 $V_{CC}$ to 1/3 $V_{CC}$ and the voltage across the capacitor is given by $1/3\ V_{CC} = 2/3\ V_{CC}\ e^{-t/RC}$

$$t = 0.69\ RC$$

$$t_{LOW} = 0.69\ R_BC$$

Notice that both $R_A$ and $R_B$ are in the charge path, but only $R_B$ is in the discharge path.

Total time $T = t_{HIGH} + t_{LOW} = 0.69\ (R_A + 2R_B)\ C.$

$$\text{So, } f = \frac{1}{T} = \frac{1.45}{(R_A + 2R_B)C}$$

Resistors $R_A$ and $R_B$ could be made variable to allow adjustment of frequency and pulse width. If $R_A = R_B$, then 50% duty cycle is achieved.]

FSK generator, pulse position Modulator are applications of the stable mode of operation of 555 Timer.

Practically a 555 timer is used in oscillators, pulse generators, ramp and square wave generator, monoshot multivibrator, burglar alarm, traffic light control and voltage monitor etc.



***OBJECTIVES***

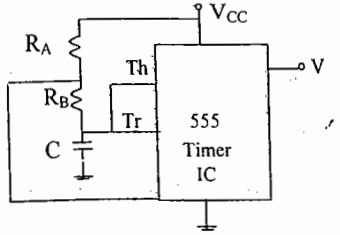
1. The circuit shows a 555 Timer IC connected as an astable multivibrator. The value of the capacitor C is 10 nF. The values of the resistors $R_A$ and $R_B$ for a frequency of 10kHz and a duty cycle of 0.75 for the output voltage waveform are ***(GATE 2003, EEE)***

a) $R_A = 3.62\ k\Omega$, $R_B = 3.62\ k\Omega$

b) $R_A = 3.62\ k\Omega$, $R_B = 7.25\ k\Omega$

c) $R_A = 7.25\ k\Omega$, $R_B = 3.62\ k\Omega$

d) $R_A = 7.25\ k\Omega$, $R_B = 7.25\ k\Omega$




Discharge

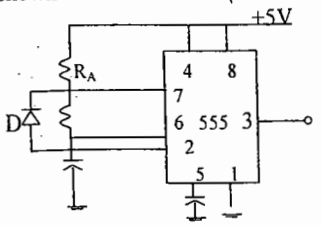
2. The function of the Diode D in the timer circuit shown below is to ***(IES 2003, ECE)***

a) Increase the charging time of C

b) Decrease the charging time of C

c) Increase the discharging time of C

d) Decrease the discharging time of C



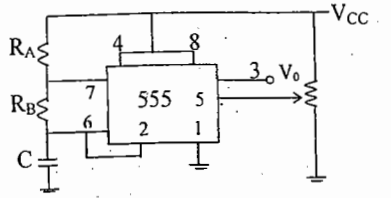

3. Circuit shown in the figure represents ***(IES '99, ECE)***

a) an astable MV

b) a monstable MV

c) VCO

d) Ramp generator



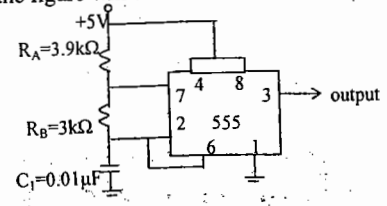

4. The output of the circuit shown in the figure will be ***(IES '97, ECE)***

a) delayed pulses

b) square waves

c) triangular waves

d) trapezoidal waves



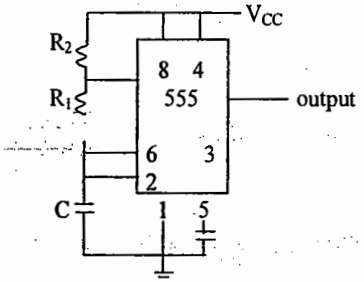
5. The given figure shown the application of 555-timer circuit as an astable multivibrator. The charging discharging time constants are respectively. *(IES '96, ECE)*

a) $R_1C$ and $R_2C$

b) $R_1C$ and $(R_1 + R_2)C$

c) $(R_1C + R_2)C$ and $R_1C$

d) $R_2C$ and $R_1C$




**Key: 1.c 2.d 3.a 4.b 5.c**

**" To win the *RACE* join the *ACE* "**

**"All the best"**

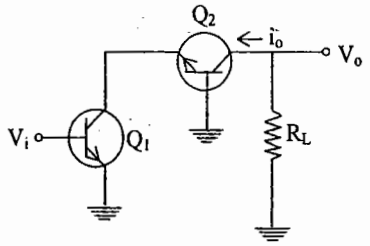
# Objective Questions Revision and Practice Set

**ONE MARK QUESTIONS**

01. The first dominant pole encountered in the frequency response of a compensated op-amp is approximately at **GATE – 1999**
(a) 5 Hz (b) 10 kHz
(c) 1 MHz (d) 100 MHz

02. Negative feedback in an amplifier **GATE – 1999**
(a) reduces gain
(b) increases frequency and phase distortions
(c) reduces bandwidth
(d) increases noise

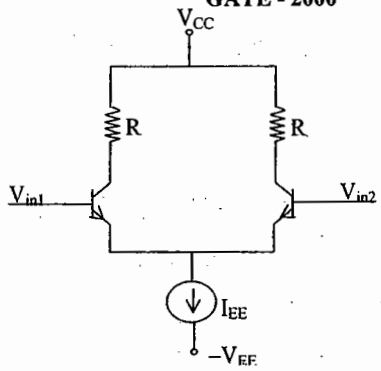
03. In the cascode amplifier shown in the figure, if the common-emitter stage ($Q_1$) has a transconductance $g_{m1}$, and the common base stage ($Q_2$) has a trasconductance $g_{m2}$, then the overall trasconductance $g(=i_o/v_i)$ of the cascode amplifier is **GATE - 1999**




(a) $g_{m1}$ (b) $g_{m2}$
(c) $g_{m1}/2$ (d) $g_{m2}/2$

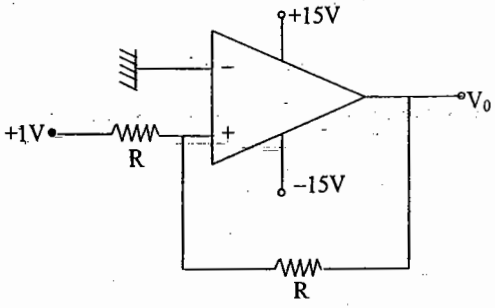
04. Crossover distortion behaviour is characteristic of **GATE - 1999**
(a) Class A output stage
(b) Class B output stage
(c) Class AB output stage
(d) Common-base output stage

05. In the differential amplifier of the figure, if the source resistance of the current source $I_{EE}$ is infinite then the common- mode gain is **GATE - 2000**




(a) zero (b) infinite
(c) indeterminate
(d) $(V_{in1} + V_{in2})/2V_T$

06. In the circuit of the figure, $V_o$ is **GATE - 2000**




(a) −1 V (b) 2V
(c) +1V (d) +15V

07. Introducing a resistor in the emitter of a common emitter amplifier stabilizes the dc operating point against variations in **GATE – 2000**

(a) only the temperature

(b) only the β of the transistor

(c) both temperature and β

(d) none of the above

08. The current gain of a bipolar transistor drops at high frequencies because of **GATE – 2000**

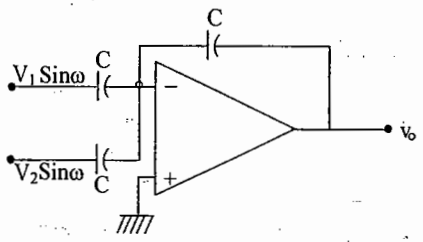
(a) transistor capacitances

(b) high current effects in the base

(c) parasitic inductive elements

(d) the Early effect

09. If the op-anp in the figure, is ideal, then $v_o$ is **GATE - 2000**




(a) zero

(b) $(V_1 - V_2)\sin\omega t$

(c) $-(V_1 + V_2)\sin\omega t$

(d) $(V_1 + V_2)\sin\omega t$

10. The most commonly used amplifier in sample and hold circuits is **GATE- 2000**

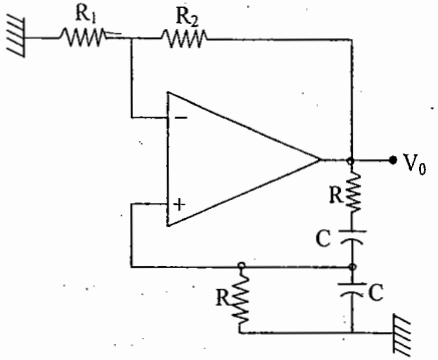
(a) a unity gain inverting amplifier

(b) a unity gain non-inverting amplifier

(c) an inverting amplifier with a gain of 10

(d) an inverting amplifier with a gain of 100

11. The configuration of the figure is a **GATE – 2000**



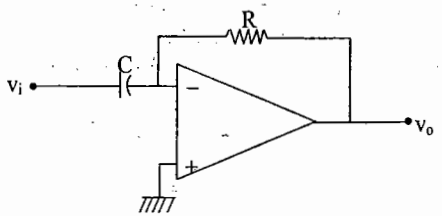

(a) precision integrator

(b) Hartley oscillator

(c) Butterworth high pass filter

(d) Wien-bridge oscillator

12. Assume that the op-amp of the figure is ideal. If $v_i$ is a triangular wave, then $v_o$ will be **GATE – 2000**




(a) square wave

(b) triangular wave

(c) parabolic wave

(d) sine wave

13 The current gain of a BJT is **GATE – 2001**

(a) $g_m r_o$ (b) $g_m/r_o$

(c) $g_m r_\pi$ (d) $g_m/r_\pi$

14. The ideal OP-AMP has the following characteristics. **GATE – 2001**

(a) $R_i = \infty, A = \infty, R_o = 0$

(b) $R_i = 0, A = \infty, R_o = 0$

(c) $R_i = \infty, A = \infty, R_o = \infty$

(d) $R_i = 0, A = \infty, R_o = \infty$



15. Consider the following two statements

**Statement 1:**
Astable multivibrator can be used for generating square wave.
**Statement 2:**
Bitable multivibrator can be used for storing binary information
**GATE – 2001**

(a) Only statement 1 is correct

(b) Only statement 2 is correct

(c) Both the statements 1 and 2 are correct

(d) Both the statements 1 and 2 are incorrect

16. In a negative feedback amplifier using voltage-series (i.e., voltage sampling, series mixing)feedback.**GATE - 2002**

(a) $R_i$ decreases and $R_o$ decreases

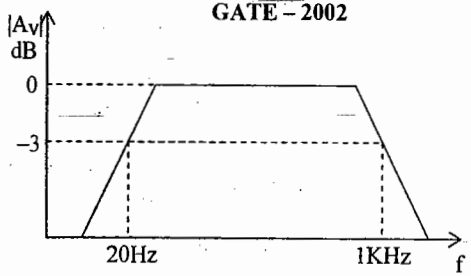
(b) $R_i$ decreases and $R_o$ increases

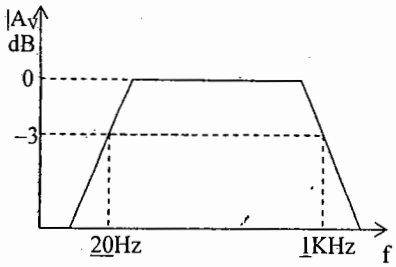
(c) $R_i$ increases and $R_o$ decreases

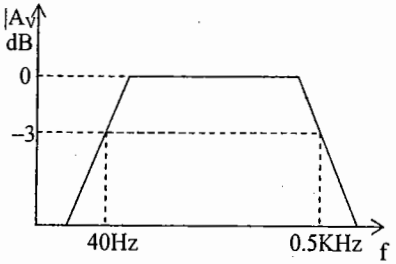
(d) $R_i$ increases and $R_o$ increases

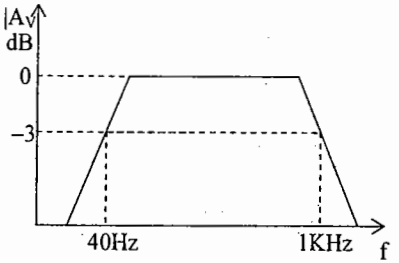
($R_i$ and $R_o$ denote the input and output resistances respectively)

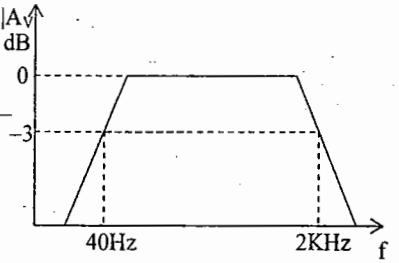
17. Three identical RC-coupled transistor amplifiers are cascaded. If each of the amplifiers has a frequency response as shown in the figure, the overall frequency response is as given in **GATE – 2002**




(a)



(b)



(c)



(d)



18. A 741-type opamp has a gain-bandwidth product of 1 MHz. A non-inverting amplifier using this opamp and having a voltage gain of 20 dB will exhibit a–3- dB bandwidth of **GATE – 2002**

(a) 50 KHz (b) 100 KHz

(c) 1000/17 KHz (d) 1000/7.07 KHz

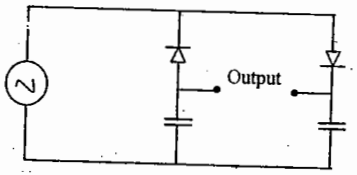
19. Choose the correct match for input resistance of various amplifier configurations shown below

| Configuration | Input resistance |
|---|---|
| CB: Common Base | LO: Low |
| CC: Common Collector | MO: Moderate |
| CE: Common Emitter | HI: high |

**GATE – 2003**

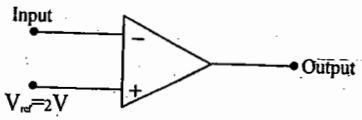
(a) CB-LO, CC-MO, CE-HI
(b) CB-LO, CC-HI, CE-MO
(c) CB-MO, CC-HI, CE-LO
(d) CB-HI, CC-LO, CE-MO

20. The circuit shown in the figure is best described as a **GATE – 2003**




(a) bridge rectifier
(b) ring modulator
(c) frequency discriminator
(d) voltage doubler

21. If the input to the ideal comparator shown in the figure is a sinusoidal signal of 8V (peak to peak) without nay DC component, then the output of the comparator has duty cycle of **GATE – 2003**




(a) 1 / 2 (b) 1 / 3
(c) 1 / 6 (d) 1 / 12

22. If the differential voltage gain and the common mode voltage gain of a deferential amplifier are 48 dB and 2 dB respectively, then its common mode rejection ratio is **GATE – 2003**

(a) 23 dB (b) 25 dB
(c) 46 dB (d) 50 dB

23. Generally, the gain of a transistor amplifier falls at high frequencies due to the **GATE – 2003**

(a) internal capacitances of the device
(b) coupling capacitor at the input
(c) skin effect
(d) coupling capacitor at the output

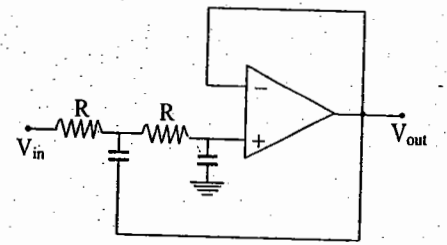
24. An ideal op-amp is an ideal **GATE – 2004**

(a) voltage controlled current source
(b) voltage controlled voltage source
(c) current controlled current source
(d) current controlled voltage source

25. Voltage series feedback(also called series-shunt feedback) results in **GATE – 2004**

(a) increase in both input and output impedances
(b) decrease in both input and output impedances
(c) increase in input impedance and decrease in output impedance
(d) decrease in input impedance and increase in output impedance

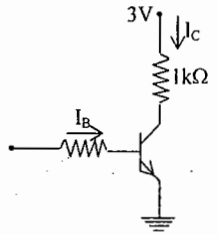
26. The circuit in the figure is a **GATE – 2004**




(a) low-pass filter
(b) high-pass filter
(c) band-pass filter
(d) band-reject filter



27. Assuming $V_{CEsat}$ = 0.2V and β = 50, the minimum base current ($I_B$) required to drive the transistor in the figure to saturation is **GATE – 2004**

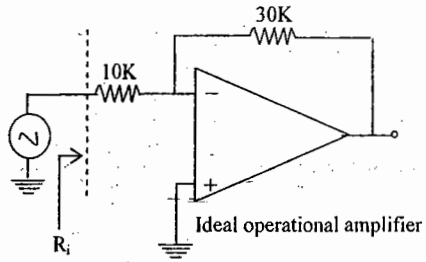



(a) 56 μA
(b) 140 mA
(c) 60 μA
(d) 3 mA

28. The effect of current shunt feedback in an amplifier is to **GATE – 2005**

(a) increase the input resistance and decrease the output resistance
(b) increase both input and output resistances
(c) decrease both input and output resistances
(d) decrease the input resistance and increase the output resistance

29. The input resistance $R_i$ of the amplifier shown in the figure is **GATE – 2005**




(a) 30/4 kΩ (b) 10 kΩ
(c) 40 kΩ (d) infinite

30. The cascade amplifier is a multistage configuration of **GATE – 2005**

(a) CC-CB (b) CE-CB
(c) CB-CC (d) CE-CC

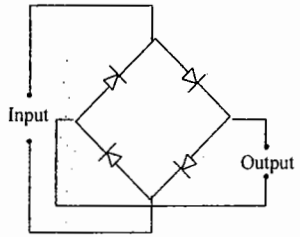
31. The input impedance ($Z_i$) and the output impedance ($Z_o$) of an ideal transconductance(voltage controlled current source) amplifier are **GATE – 2006**

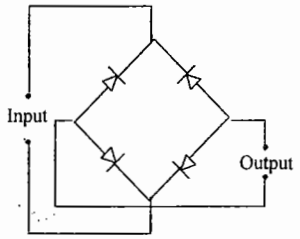
(a) $Z_i = 0, Z_o = 0$ (b) $Z_i = 0, Z_o = \infty$
(c) $Z_i = \infty, Z_o = 0$ (d) $Z_i = \infty, Z_o = \infty$

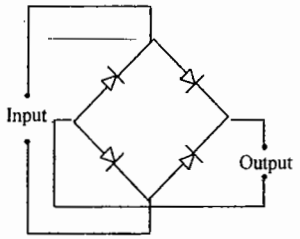
32. An n-channel depletion MOSFET has following two points on its $I_D - V_{GS}$ curve:
(i) $V_{GS} = 0$ at $I_D$ = 12 mA and
(ii) $V_{GS} = -6$ Volts at $I_D = 0$
Which of the following Q-points will give the highest trans-conductance gain for small signals? **GATE – 2006**

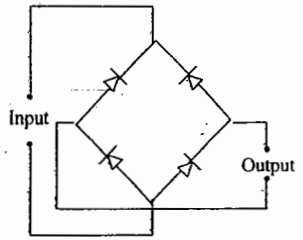
(a) $V_{GS} = -6$ Volts (b) $V_{GS} = -3$ Volts
(c) $V_{GS} = 0$ Volts (d) $V_{GS} = 3$ Volts

33. The correct full wave rectifier is **GATE – 2007**

(a)


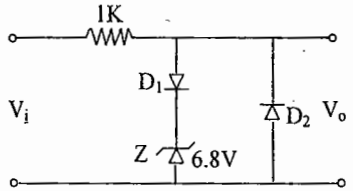

(b)



(c)



(d)


34. In a trasconductance amplifier, it is desirable to have **GATE - 2007**
(a) a large input resistance and large output resistance
(b) a large input resistance and a small output resistance
(c) a small input resistance and a large output resistance
(d) a small input resistance and a small output resistance

35. In the following limiter circuit, an input voltage $V_i = 10 \sin 100\pi t$ is applied. Assume that the diode drop is 0.7 V when it is forward biased. The Zener breakdown voltage is 6.8 V.




The maximum and minimum values of the output voltage respectively are
**GATE – 2008**
(a) 6.1 V, –0.7 V (b) 0.7 V, –7.5 V
(c) 7.5 V, –0.7 V (d) 7.5 V, –7.5 V

**KEY**

| | | | | | |
|---|---|---|---|---|---|
| 1. a | 2. b | 3. a | 4. b | 5.a | 6. d |
| 7. c | 8. a | 9. c | 10.b | 11.d | 12.a |
| 13. c | 14. a | 15. c | 16. c | 17. a | 18. b |
| 19. b | 20.d | 21. b | 22. c | 23. a | 24. b |
| 25. c | 26. a | 27. a | 28. d | 29. b | 30. b |
| 31. d | 32. d | 33. c | 34. a | 35. c | |



**TWO MARKS QUESTIONS**

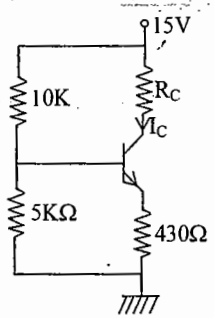
01. An npn transistor (with $C_\mu = 0.3$ pF) has a unity-gain cutoff frequency $f_T$ of 400 MHz at dc bias current $I_C = 1$mA. The value of its $C_\mu$ (in pF) is approximately ($V_T = 26$mV)
**GATE – 1999**
(a) 15 (b) 30
(c) 50 (d) 96

02. An amplifier has an open-loop gain of 100, an input impedance of 1kΩ, and an output impedance of 100Ω. A feedback network with a feedback factor of 0.99 is connected to the amplifier in a voltage series feedback mode. The new input and output impedances respectively, are
**GATE – 1999**
(a) 10 Ω and 1 Ω
(b) 10 Ω and 10 kΩ
(c) 100 kΩ and 1 Ω
(d) 100 kΩ and 10 kΩ

03. A dc power supply has a no-load voltage of 30 V, and a full-load voltage of 25 V at a full-load current of 1 A. Its output resistance and load regulation respectively, are
**GATE – 1999**
(a) 5 Ω and 20% (b) 25 Ω and 20%
(c) 5 Ω and 16.7% (d) 25 Ω and 16.7%

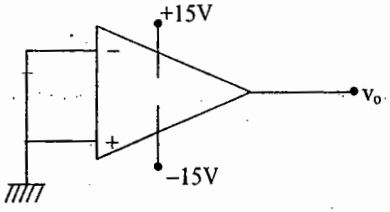
04. An amplifier is assumed to have a single-pole high-frequency transfer function. The rise time of its output response to a step function input is 35 nsec. The upper-3 dB frequency (in MHz) for the amplifier to a sinusoidal input is approximately at
**GATE – 1999**
(a) 4.55 (b) 10
(c) 20 (d) 28.6

05. In the circuit of the figure, assume that the transistor is in the active region. It has a large β and its base-emitter voltage is 0.7V. The value of $I_c$ is
**GATE – 2000**




(a) Indeterminate since $R_c$ is not given
(b) 1 mA
(c) 5 mA
(d) 10 mA

06. If the op-amp in the figure has an input offset voltage of 5 mV and an open-loop voltage gain of 10,000, then $v_o$ will be
**GATE – 2000**



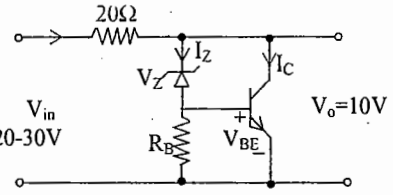

(a) 0 V
(b) 5 mV
(c) +15 V or –15 V
(d) +50V or –50 V

07. An npn BJT has $g_m$ = 38 mA/V, $C_\mu = 10^{-14}$F, $C_\pi = 4 \times 10^{-13}$ F, and DC current gain $\beta_o$ = 90. For this transistor $f_T$ and $f_\beta$ are

**GATE – 2001**

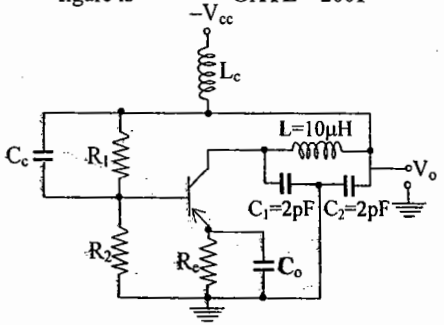
(a) $f_T = 1.64 \times 10^8$ Hz and $f_\beta = 1.47 \times 10^{10}$ Hz
(b) $f_T = 1.47 \times 10^{10}$ Hz and $f_\beta = 1.64 \times 10^8$ Hz
(c) $f_T = 1.33 \times 10^{12}$ Hz and $f_\beta = 1.47 \times 10^{10}$ Hz
(d) $f_T = 1.47 \times 10^{10}$ Hz and $f_\beta = 1.33 \times 10^{12}$ Hz

08. The transistor shunt regulator shown in the figure has a regulated output voltage of 10 V, when the input varies form 20 V to 30V. The relevant parameters for the zener diode and the transistor are: $V_z$ = 9.5 V, $V_{BE}$ = 0.3V, $\beta$ = 99. Neglect the current through $R_B$. Then the maximum power dissipated in the zener diode ($P_Z$) and the transistor ($P_T$) are **GATE – 2001**




(a) $P_Z$ = 75mW, $P_T$ = 7.9 W
(b) $P_Z$ = 85mW, $P_T$ = 8.9 W
(c) $P_Z$ = 95mW, $P_T$ = 9.9 W
(d) $P_Z$ = 115mW, $P_T$ = 11.9 W

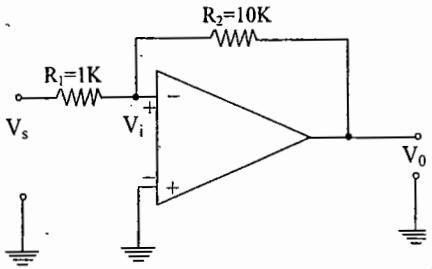
09. The oscillator circuit shown in the figure is **GATE – 2001**




(a) Hartley oscillator with $f_{oscillation}$ = 79.6 MHz
(b) Colpitts oscillator with $f_{oscillation}$ = 79.6 MHz
(c) Hartley oscillator with $f_{oscillation}$ = 159.2 MHz
(d) Colpitts oscillator with $f_{oscillation}$ = 159.2 MHz

10. The inverting OP-AMP shown in the figure has an open-loop gain of 100. The closed-loop gain $\frac{V_o}{V_s}$ is

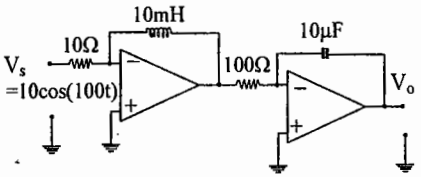
**GATE – 2001**




(a) –8 (b) –9
(c) –10 (d) –11

11. In the figure assume the OP-AMPs to be ideal. The output $V_o$ of the circuit is

**GATE – 2001**




(a) 10cos(100t) (b) $10\int_0^t \cos(100\tau)d\tau$

(c) $10^{-4}\int_0^t \cos(100\tau)d\tau$

(d) $10^{-4}\frac{d}{dt}\cos(100t)$



12. An amplifier using an opamp with a slew-rate SR=1 V/μsec has a gain of 40 dB. If this amplifier has to faithfully amplify sinusoidal signals form dc to 20 KHz without introducing any slew-rate induced distortion, then the input signal level must not exceed.

**GATE – 2002**

(a) 795 mV (b) 395 mV
(c) 79.5 mV (d) 39.5 mV

13. An amplifier without feedback has a voltage gain of 50, input resistance of 1KΩ and output resistance of 2.5 k Ω. The input resistance of the current-shunt negative feedback amplifier using the above amplifier with a feedback factor of 0.2 is

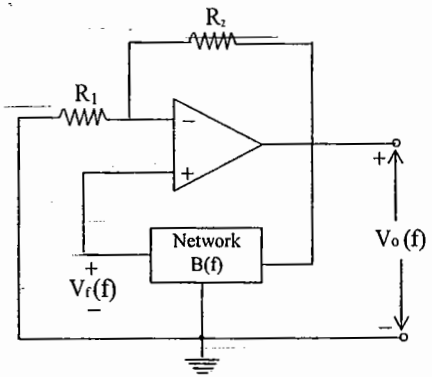
**GATE – 2003**

(a) 1/11 KΩ (b) 1/5 KΩ
(c) 5 KΩ (d) 11 KΩ

14. The circuit in the figure employs positive feedback and is intended to generate sinusoidal oscillation. If at a frequency $f_o$, then to sustain oscillation at this frequency

$$B(f) = \frac{V_f(f)}{V_o(f)} = \frac{1}{6}\angle 0°$$

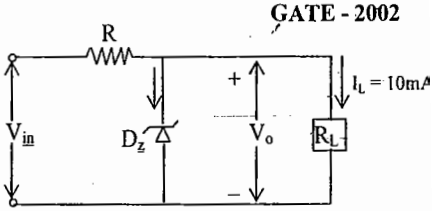
**GATE - 2002**




(a) $R_2 = 5\,R_1$ (b) $R_2 = 6\,R_1$
(c) $R_2 = \frac{R_1}{6}$ (d) $R_2 = \frac{R_1}{5}$

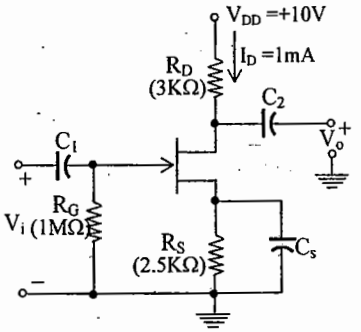
15. A zener diode regulator in the figure is to be designed to meet the specifications: $I_L$ = 10mA, $V_o$ = 10 V and $V_{in}$ varies from 30 V to 50 V. The zener diode has $V_Z$ = 10V and $I_{zk}$ (knee current) = 1mA. For satisfactory operation.

**GATE - 2002**




(a) R ≤ 1800 Ω
(b) 2000 Ω ≤ R ≤ 2200 Ω
(c) 3700 Ω ≤ R ≤4000Ω
(d) R > 4000Ω

16. The voltage gain $A_V = V_0 / V_i$ of the JFET amplifier shown in the figure is **GATE - 2002**

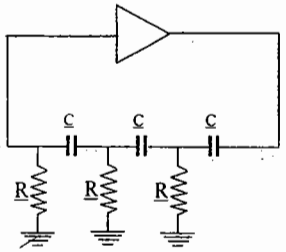



$I_{DSS}$ = 10mA $V_p$ = –5 V
(Assume $C_1$, $C_2$ and $C_s$ to be very large)

(a) +18 (b) –18
(c) +6 (d) –6

17. The oscillator circuit shown in the figure has an ideal inverting amplifier. Its frequency of oscillation (in Hz) is

**GATE – 2003**



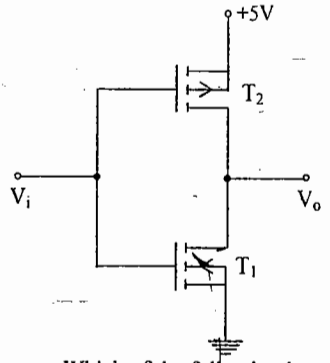

(a) $\frac{1}{(2\pi\sqrt{6}RC)}$ (b) $\frac{1}{(2\pi 2\pi R}$

(c) $\frac{1}{(\sqrt{6}RC)}$ (d) $\frac{\sqrt{6}}{(2\pi 2\pi R}$

18. Consider the following statements in connection with the CMOS inverter in the figure, where both the MOSFETs are of enhancement type and both have a threshold voltage of 2V.

**Statement 1:** $T_1$ conducts when $Vi \geq 2V$.

**Statement 2:** $T_1$ is always in saturation when $V_o = 0V$.



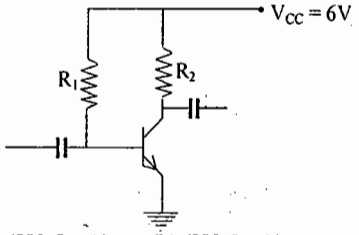

Which of the following is correct?

**GATE - 2002**

(a) Only Statement 1 is TRUE
(b) Only Statement 2 is TRUE
(c) Both the Statements are TRUE
(d) Both the Statements are FALSE

19. In the amplifier circuit shown in the figure, the values of $R_1$ and $R_2$ are such that the transistor is operating at $V_{CE} = 3V$ and $I_C = 1.5$ mA when its $\beta$ is 150. For a transistor with $\beta$ of 200, the operating point ($V_{CE}$, $I_C$) is

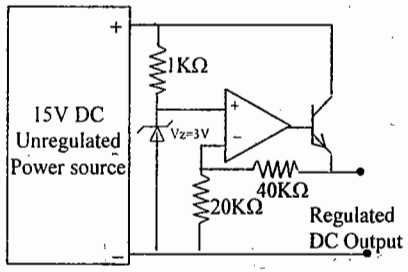
**GATE – 2003**




(a) (2V, 2mA) (b) (3V, 2mA)
(c) (4V, 2mA) (d) (4V, 1mA)

20. The output voltage of the regulated power supply shown in the figure is

**GATE – 2003**




(a) 3 V (b) 6 V
(c) 9 V (d) 12 V

21. The action of a JFET in its equivalent circuit can best be represented as a

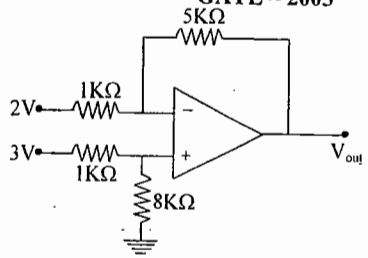
**GATE – 2003**

(a) Current Controlled Current Source
(b) Current Controlled Voltage Source
(c) Voltage Controlled Voltage Source
(d) Voltage Controlled Current Source



22. If the op-amp in the figure is ideal, the output voltage $V_{out}$ will be equal to

**GATE – 2003**




(a) 1 V (b) 6 V
(c) 14 V (d) 17 V

23. Three identical amplifiers with each one having a voltage gain of 50, input resistance of 1 KΩ and output resistance of 250Ω, are cascaded. The open circuit voltage gain of the combined amplifier is

**GATE – 2003**

(a) 49 dB (b) 51 dB
(c) 98 dB (d) 102 dB

24. An ideal sawtooth voltage waveform of frequency 500 Hz and amplitude 3 V is generated by charging a capacitor of 2μF in every cycle. The charging requires

**GATE – 2003**

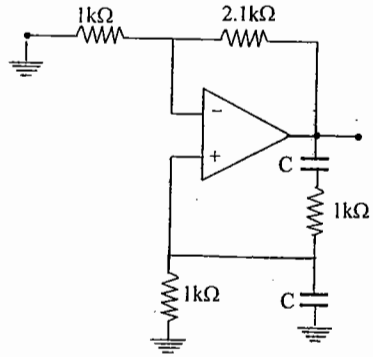
(a) constant voltage source of 3 V for 1 ms
(b) constant voltage source of 3 V for 2 ms
(c) constant current source of 3 mA for 1 ms
(d) constant current source of 3 mA for 2 ms

25. A bipolar transistor is operating in the active region with a collector current of 1 mA. Assuming that $\beta$ of the transistor is 100 and the thermal voltage ($V_T$) is 25 mV, the transconducatance ($g_m$) and the input resistance ($r_\pi$) of the transistor in the common emitter configuration, are

**GATE – 2004**

(a) $g_m = 25$mA/V and $r_\pi = 15.625$ kΩ
(b) $g_m = 40$mA/V and $r_\pi = 4.0$ kΩ
(c) $g_m = 25$mA/V and $r_\pi = 2.5$ kΩ
(d) $g_m = 40$mA/V and $r_\pi = 2.5$ kΩ

26. The value of C required for sinusoidal oscillations of frequency 1 kHz in the circuit of the figure is **GATE- 2004**

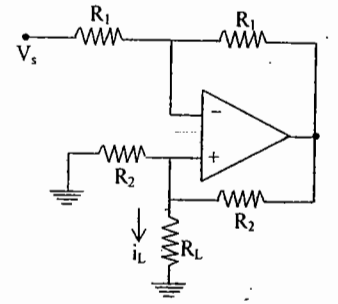



(a) $\frac{1}{2\pi}\mu F$ (b) $2\pi\ \mu F$

(c) $\frac{1}{2\pi\sqrt{6}}\mu F$ (d) $2\pi\sqrt{6}\,\mu F$

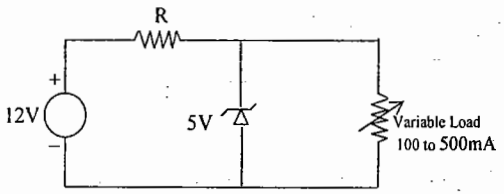
27. In the op-amp circuit given in the figure, the load current $i_L$ is

**GATE - 2004**




(a) $-\frac{V_s}{R_2}$ (b) $\frac{V_s}{R_2}$ (c) $-\frac{V_s}{R_L}$ (d) $\frac{V_s}{R_L}$

28. In the voltage regulator shown in the figure, the load current can vary from 100 mA to 500 mA. Assuming that the Zener diode is ideal (i.e., the Zener knee current is negligibly small and Zener resistance is zero in the breakdown region), the value of R is
**GATE – 2004**




(a) 7Ω (b) 70Ω
(c) 70/3 Ω (d) 14Ω

29. In a full-wave rectifier using two ideal diodes, $V_{dc}$ and $V_m$ are the dc and peak values of the voltage respectively across a resistive load. If PIV is the peak inverse voltage of the diode, then the appropriate relationships for this rectifier are **GATE – 2004**

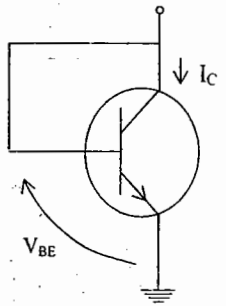
(a) $V_{dc} = \frac{V_m}{\pi}, PIV = 2V_m$

(b) $V_{dc} = 2\frac{V_m}{\pi}, PIV = 2V_m$

(c) $V_{dc} = 2\frac{V_m}{\pi}, PIV = V_m$

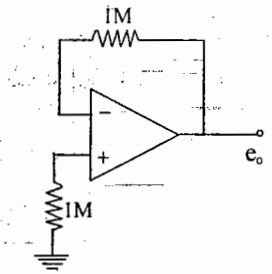
(d) $V_{dc} = \frac{V_m}{\pi}, PIV = V_m$

30. For an npn transistor connected as shown in the figure, $V_{BE} = 0.7$ volts. Given that reverse saturation current of the junction at room temperature $300^o$ K is $10^{-13}$ A, the emitter current is
**GATE – 2005**




(a) 30 mA (b) 39 mA
(c) 49 mA (d) 20 mA

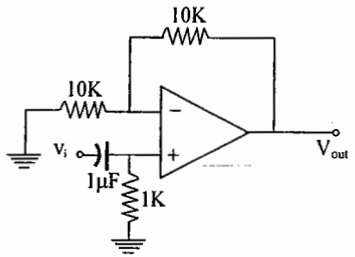
31. The voltage $e_0$ indicated in the figure has been measured by an ideal voltmeter. Which of the following can be calculated?
**GATE – 2005**




(a) Bias current of the inverting input only
(b) Bias current of the inverting and non- inverting inputs only
(c) Input offset current only
(d) Both the bias currents and the input offset current

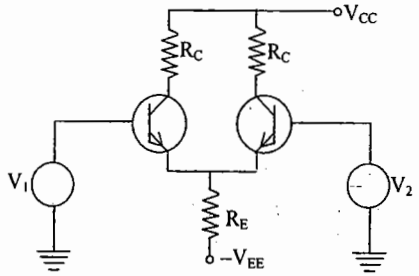


32. The op-amp circuit shown in the figure is a filter. The type of filter and its cut-off frequency are respectively
**GATE – 2005**



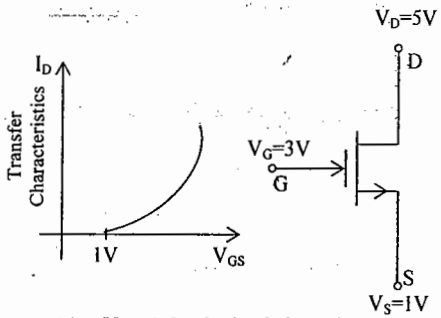

(a) high pass, 1000 rad/sec.
(b) low pass, 1000 rad/sec.
(c) high pass, 10000 rad/sec.
(d) low pass, 10000 rad/sec.

33. In an ideal differential amplifier shown in the figure, a large value of $R_E$
**GATE – 2005**



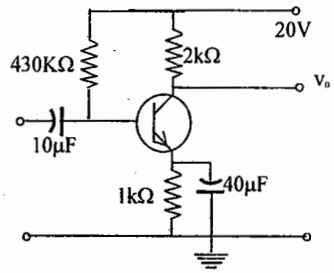

(a) increases both the differential and common-mode gains
(b) increases the common-mode gain only
(c) decreases the differential-mode gain only
(d) decreases the common-mode gain only.

34. For an n-channel MOSFET and its transfer curve shown in the figure, the threshold voltage is **GATE – 2005**




(a) 1 V and the device is in active region
(b) -1 V and the device is in saturation region
(c) 1 V and the device is in saturation region
(d) -1 V and the device is in active region.

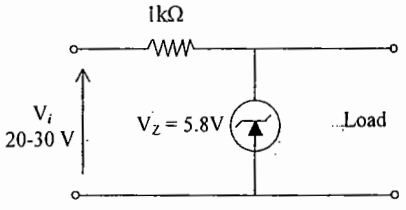
35. The circuit using a BJT with $\beta = 50$ and $V_{BE} = 0.7$ V is shown in the figure. The base current $I_B$ and collector voltage $V_C$ are respectively
**GATE - 2005**




(a) 43 μA and 11.4 Volts
(b) 40 μA and 16 Volts
(c) 45 μA and 11 Volts
(d) 50 μA and 10 Volts

36. The zener diode in the regulator circuit shown in the figure has a zener voltage of 5.8 volts and a zener knee current of 0.5 mA. The maximum load current drawn form this circuit ensuring proper functioning over the input voltage range between 20 and 30 volts is

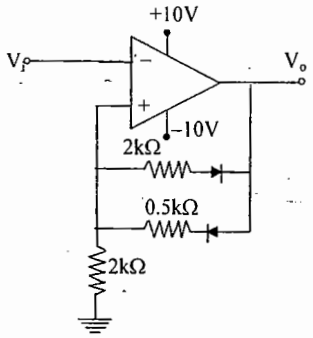
**GATE – 2005**



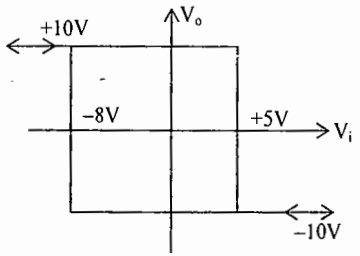

(a) 23.7 mA (b) 14.2 mA
(c) 13.7 mA (d) 24.2 mA

37. Given the ideal operational amplifier circuit shown in the figure indicate the correct transfer characteristics assuming ideal diodes with zero cut-in voltage.

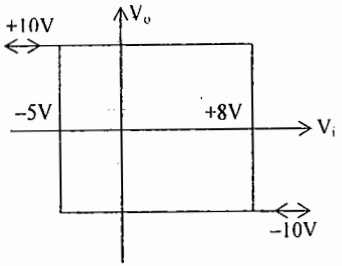
**GATE – 2005**



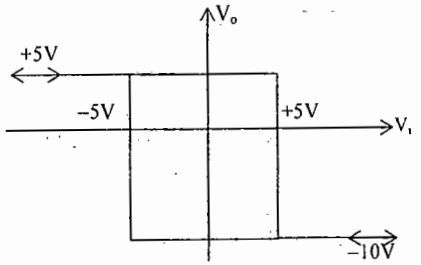

(a)



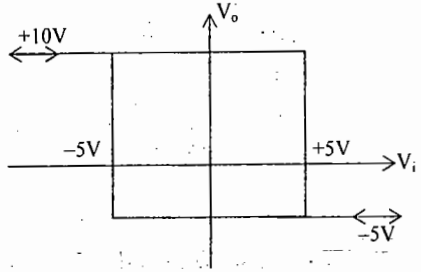

(b)




(c)




(d)

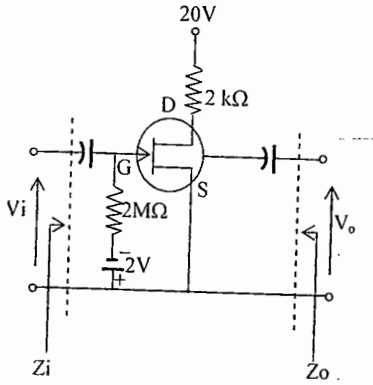





**Common Data Questions 38, 39, 40**

Given, $r_d$ = 20 kΩ, $I_{DSS}$ = 10 mA, $V_P$ = −8V

**GATE - 2005**




38. $Z_i$ and $Z_o$ of the circuit are respectively

**GATE – 2005**

(a) 2 MΩ and 2 kΩ

(b) 2 MΩ and 20/11 kΩ

(c) infinity and 2 kΩ

(d) infinity and 20/11 kΩ,

39. $I_D$ and $V_{DS}$ under DC conditions are respectively **GATE – 2005**

(a) 5.625 mA and 8.75 V

(b) 7.500 mA and 5.00 V

(c) 4.500 mA and 11.00 V

(d) 6.250 mA and 7.50 V

40. Transconductance in milli-Siemens (mS) and voltage gain of the amplifier are respectively. **GATE – 2005**

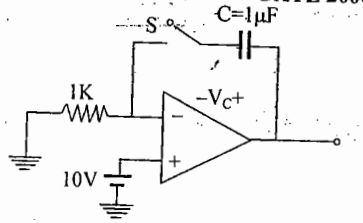
(a) 1.875 mS and 3.41

(b) 1.875 mS and -3.41

(c) 3.3 mS and -6

(d) 3.3 mS and 6

41. For the circuit shown in the following figure, the capacitor C is initially uncharged. At t = 0, the switch S is closed. The voltage $V_C$ across the capacitor at t = 1 ms is **GATE 2006**

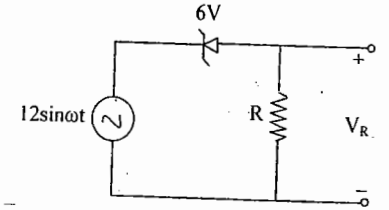



In the figure shown above, the OP-AMP is supplied with ± 15V.

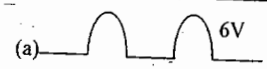
(a) 0 Volt (b) 6.3 Volts
(c) 9.45 Volts (d) 10 Volts

42. For the circuit shown below, assume that the zener diode is ideal with a breakdown voltage of 6 volts. The waveform observed across R is

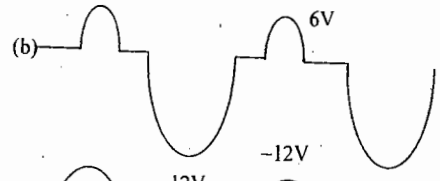
**GATE - 2006**



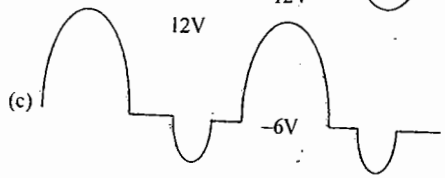

(a)



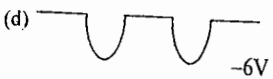

(b)




(c)




(d)

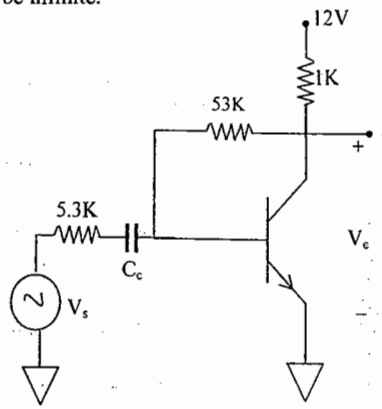


**Common Data for Questions 43, 44 & 45.**

In the transistor amplifier circuit shown in the figure below, the transistor has the following parameters:

$\beta_{DC} = 60$, $V_{BE} = 0.7$ V, $h_{ie} \to \infty$, $h_{fe} \to \infty$

The capacitance $C_C$ can be assumed to be infinite.




In the figure above, the ground has been shown by the symbol ∇

**GATE - 2006**

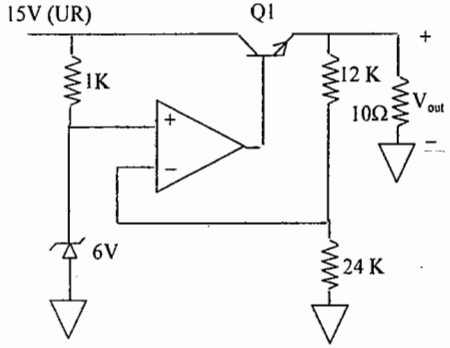
43. Under the DC conditions, the collector-to-emitter voltage drop is
(a) 4.8 Volts (b) 5.3 Volts
(c) 6.0 Volts (d) 6.6 Volts

44. If $\beta_{DC}$ is increased by 10%, the collector-to-emitter voltage drop
(a) increases by less than or equal to 10%
(b) decreases by less than or equal to 10%
(c) increases by more than 10%
(d) decreases by more than 10%

45. The small-signal gain of the amplifier $V_o/V_s$ is **GATE – 2006**
(a) -10 (b) -5.3
(c) 5.3 (d) 10

**Statement for Linked Answer 46 & 47.**

A regulated power supply, shown in figure below, has an unregulated input (UR) of 15 V and generates a regulated output $V_{out}$. Use the component values shown in the figure.



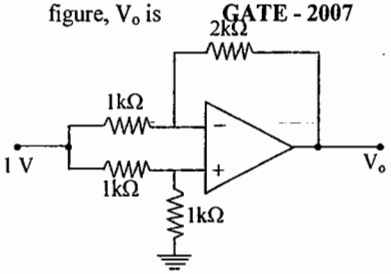

In the figure above, the ground has been shown by the symbol ∇

**GATE - 2006**

46. The power dissipation across the transistor Q1 shown in the figure is
(a) 4.8 Watts (b) 5.0 Watts
(c) 5.4 Watts (d) 6.0 Watts

47. If the unregulated voltage increases by 20% the power dissipation across the transistor Q1.
(a) increases by 20%
(b) increases by 50%
(c) remains unchanged
(d) decreases by 20%

48. For the Op-Amp circuit shown in the figure, $V_o$ is **GATE - 2007**

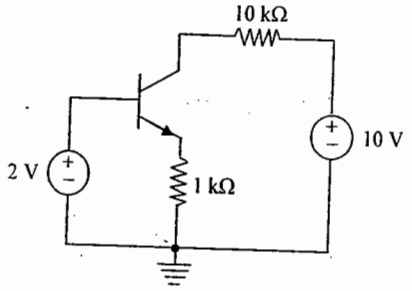



(a) –2V (b) –1 V
(c) –0.5 V (d) 0.5 V



49. The DC current gain (β) of a BJT is 50. Assuming that the emitter injection efficiency is 0.995, the base transport factor is **GATE – 2007**
(a) 0.980 (b) 0.985
(c) 0.990 (d) 0.995

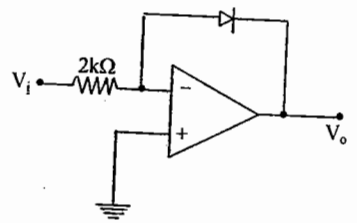
50. For the BJT circuit shown, assume that the β of the transistor is very large and $V_{BE} = 0.7$ V. The mode of operation of the BJT is **GATE – 2007**




(a) cut-off (b) saturation
(c) normal active (d) reverse active

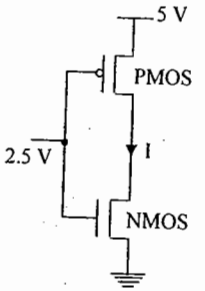
51. In the Op-Amp circuit shown, assume that the diode current follows the equation $I = I_s \exp(V/V_T)$. For $V_i = 2$ V, $V_o = V_{01}$, and for $V_i = 4$ V, $V_o = V_{02}$. The relationship between $V_{01}$ and $V_{02}$ is

**GATE – 2007**



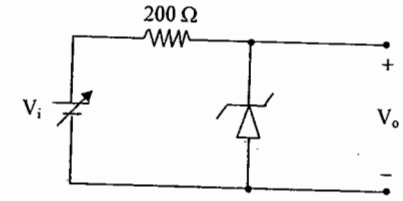

(a) $V_{02} = \sqrt{2}\, V_{01}$
(b) $V_{02} = e^2 V_{01}$
(c) $V_{02} = V_{01} \ln 2$
(d) $V_{01} - V_{02} = V_T \ln 2$

52. In the C MOS inverter circuit shown if the trasconductacnce parameters of the NMOS and PMOS transistors are $k_n = k_p = \mu_n C_{ox}$ $\frac{W_n}{L_n} = \mu_p C_{ox} \frac{W_p}{L_p} = 40\mu A/V^2$ and their threshold voltages are $V_{THn} = |V_{THp}| =$ 1 V, the current I is **GATE - 2007**




(a) 0 A (b) 25 μA
(c) 45 μA (d) 90 μA

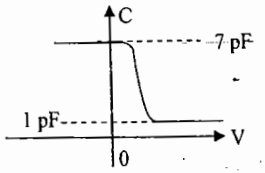
53. For the Zener diode shown in the figure, the Zener voltage at knee is 7 V, the knee current is negligible and the Zener dynamic resistance is 10 Ω. If the input voltage ($V_i$) range is from 10 to 16V, the output voltage ($V_o$) ranges from **GATE – 2007**




(a) 7.00 to 7.29 V (b) 7.14 to 7.29 V
(c) 7.14 to 7.43 V (d) 7.29 to 7.43 V

**Common Data for Questions 54, 55, 56 :**

The figure shows the high-frequency capacitance-voltage (C-V) characteristics of a Metal/$SiO_2$/silicon (MOS) capacitor having an area of 1 x $10^{-4}$ $cm^2$. Assume that the permittivities ( $\varepsilon_o\varepsilon_r$) of silicon and $SiO_2$ are 1 x $10^{-12}$ F/cm and 3.5 x $10^{-13}$ F/cm respectively.



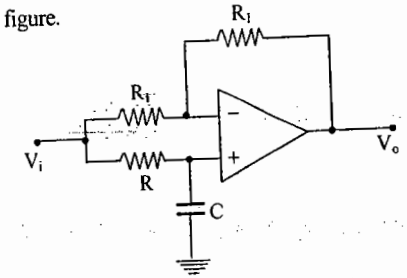

54. The gate oxide thickness in the MOS capacitor is **GATE – 2007**
(a) 50 nm (b) 143 nm
(c) 350 nm (d) 1 μm

55. The maximum depletion layer width in silicon is **GATE – 2007**
(a) 0.143 μm (b) 0.857 μm
(c) 1 μm (d) 1.143 μm

56. Consider the following statements about the C-V characteristics plot:
**S1 :** The MOS capacitor has as n-type substrate.
**S2 :** If positive charges are introduced in the oxide, the C-V plot will shift to the left.
Then which of the following is true?
**GATE - 2007**
(a) Both S1 and S2 are true
(b) S1 is true and S2 is false
(c) S1 is false and S2 is true
(d) Both S1 and S2 are false

**Statement for Linked Answer Questions 57 & 58 :**

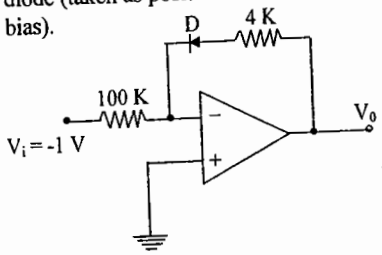
Consider the Op-Amp circuit shown in the figure.




57. The transfer function $V_o(s)/V_i(s)$ is **GATE -2007**
(a) $\frac{1-sRC}{1+sRC}$ (b) $\frac{1+sRC}{1-sRC}$
(c) $\frac{1}{1-sRC}$ (d) $\frac{1}{1+sRC}$

58. If $V_i = V_1 \sin(\omega t)$ and $V_o = V_2 V_1 \sin(\omega t+\phi)$, then the minimum and maximum values of $\phi$ (in radians) are respectively **GATE – 2007**
(a) $-\pi/2$ and $\pi/2$ (b) 0 and $\pi/2$
(c) $-\pi$ and 0 (d) $-\pi/2$ and 0

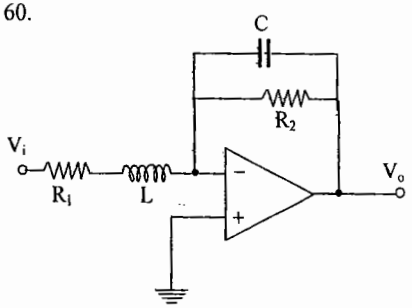
59. Consider the following circuit using an ideal OPAMP. The I-V characteristics of the diode is described by the relation $I = I_o\left(e^{\frac{V}{V_T}} - 1\right)$ where $V_T$= 25mV, $I_o$ = 1 μA and $V$ is the voltage across the diode (taken as positive for forward bias).




For an input voltage $V_i$ = –1 V, the output voltage $V_o$ is **GATE – 2008**
(a) 0 V (b) 0.1 V
(c) 0.7 V (d) 1.1 V

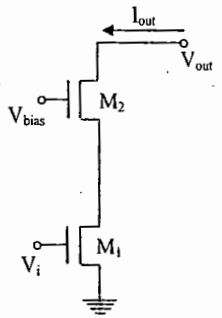


60.



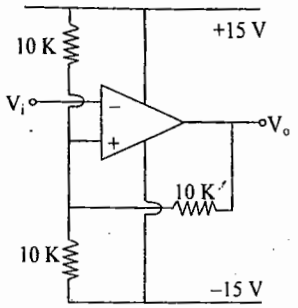

The OPAMP circuit shown above represents a **GATE – 2008**
(a) high pass filter
(b) low pass filter
(c) band pass filter
(d) band reject filter

51. Two identical NMOS transistors M1 and M2 are connected as shown below. $V_{bias}$ is chosen so that both transistors are in saturation. The equivalent $g_m$ of the pair is defined to be $\frac{\partial I_{out}}{\partial V_i}$ at constant $V_{out}$.




The equivalent $g_m$ of the pair is **GATE – 2008**
(a) the sum of individual $g_m$'s of the transistors
(b) the product of individual $g_m$'s of the transistors
(c) nearly equal to the $g_m$ of M1
(d) nearly equal to $g_m/g_o$ of M2

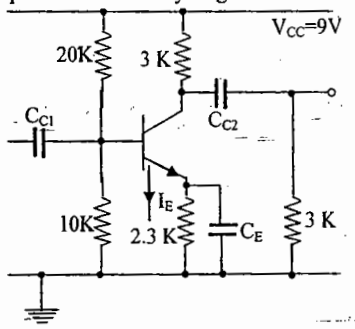
62. Consider the Schmidt trigger circuit shown below.




A triangular wave which goes form 12 V to 12 V is applied to the inverting input of the OPAMP. Assume that the output of the OPAMP swings from +15 V to –15 V. The voltage at the non-inverting input switches between. **GATE – 2008**
(a) –12 V and +12 V
(b) –7.5 and +7.5 V
(c) –5 V and +5 V
(d) 0 V and 5 V

**Statement for linked Answer Questions 63 and 64:**

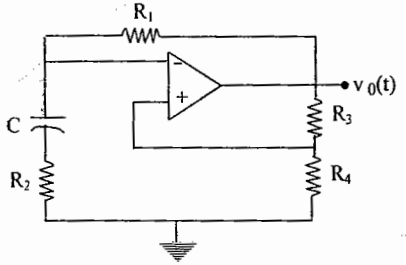
In the following transistor circuit, $V_{BE}$ = 0.7V, $r_e$ = 25mV/$I_E$, and β and all the capacitances are very large.




63. The value of DC current $I_E$ is
(a) 1 mA (b) 2 mA
(c) 5 mA (d) 10 mA

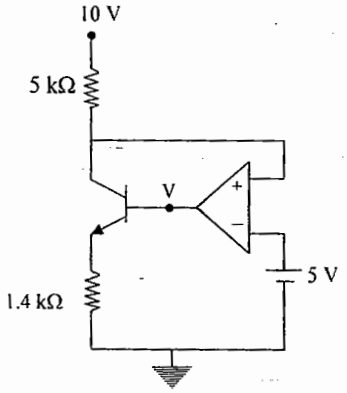
64. The mid-band voltage gain of the amplifier is approximately.
(a) –180 (b) –120
(c) –90 (d) –60

65. In the following astable multivibrator circuit, which properties of $v_0(t)$ depend on $R_2$? **GATE - 2009**



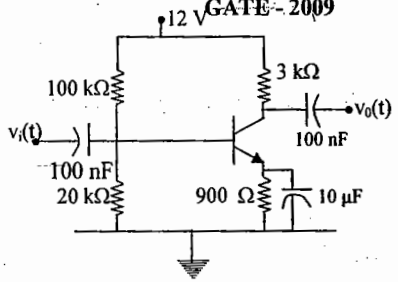

(a) Only the frequency
(b) Only the amplitude
(c) both the amplitude and the frequency
(d) Neither the amplitude nor the frequency

66. In the circuit shown below, the op-amp is ideal, the transistor has $V_{BE} = 0.6$ V and $\beta = 150$. Decide whether the feedback in the circuit is positive or negative and determine the voltage V at the output of the op-amp.
**GATE - 2009**




(a) Positive feedback, V = 10 V
(b) Positive feedback, V = 0 V
(c) Negative feedback, V = 5 V
(d) Negative feedback, V = 2 V

67. A small signal source $v_i(t) = A \cos 20t + B \sin 10^6 t$ is applied to a transistor amplifier as shown below. The transistor has $\beta = 150$ and $h_{ie} = 3$ kΩ. Which expression best approximates $v_0(t)$?
**GATE - 2009**




(a) $v_0(t) = -1500(A \cos 20t + B \sin 10^6 t)$
(b) $v_0(t) = -150(A \cos 20t + B \sin 10^6 t)$
(c) $v_0(t) = -1500\ B \sin 10^6 t$
(d) $v_0(t) = -150\ B \sin 10^6 t$

68. Which one of the following type of negative feedback increases the input resistance and decreases the output resistance of an amplifier? **IES 2009**
(a) Current series feedback
(b) Voltage series feedback
(c) Current shunt feedback
(d) Voltage shunt feedback

69. Consider a 565 PLL with $R_T = 10$ k Ω and $C_T = 0.01$ μ F. What is the output frequency of the $V_{CO}$ ? **IES 2009**
(a) 10 kHz (b) 5 kHz
(c) 2.5 kHz (d) 1.25 kHz

**KEY**

| | | | | | |
|---|---|---|---|---|---|
| 1. a | 2. c | 3. b | 4. b | 5. d | 6. c |
| 7. b | 8. c | 9. b | 10. b | 11. a | 12.c |
| 13. a | 14. a | 15. a | 16. d | 17. a | 18.c |
| 19. a | 20.c | 21.d | 22. b | 23. c | 24. d |
| 25. d | 26. a | 27. a | 28. d | 29. b | 30.c |
| 31.c | 32.a | 33. d | 34. c | 35. b | 36. a |
| 37. b | 38. b | 39. a | 40. b | 41. d | 42. b |
| 43. c | 44. b | 45. a | 46. d | 47. b | 48. c |
| 49. b | 50. b | 51. d | 52. d | 53. c | 54.a |
| 55. c | 56. d | 57. a | 58. c | 59. b | 60. b |
| 61. c | 62. c | 63. a | 64. d | 65. | 66. |
| 67. | 68. | 69. | | | |

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